OEM Integration Guide

Overview

The ICE Platform consists of daughter modules that are connected together through a common power and communications bus. The daughter modules can be controlled by a master controller (ICE-MC1) that performs power regulation, monitoring, and communications interfacing. All the circuit boards are designed to the same template so that they can be stacked together to form a board-to-board bus without the use of an additional backplane. An example of this stacking is shown below in figure 1.

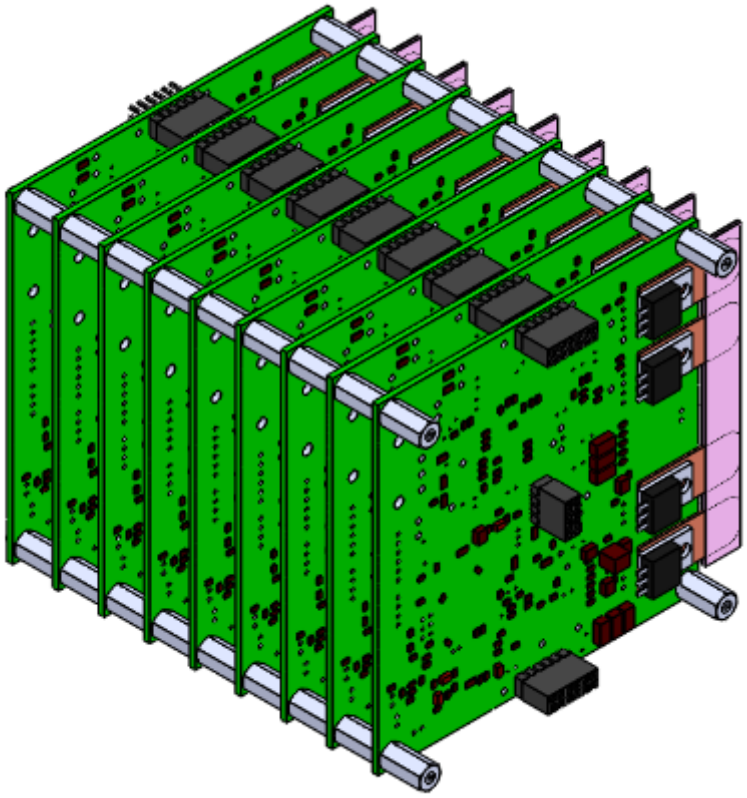


Fig. 1: ICE daughter modules stacked together.

Each PCB has common locations for mounting holes, board-to-board interconnects, I/O connectors, and heatsinking tabs. Once the boards are stacked together, each board can be addressed and communicated with through a serial I^2C bus (see this page for I^2C details). Each daughter board can have a specific I^2C address set via dip switches on each circuit board and the master controller (ICE-MC1) can route commands directly to each board. The master controller also routes and manages the power bus going to each board. Up to 8 I^2C addresses can be assigned, allowing up to 8 daughter boards to be connected to a single master controller (for a total stack of 9 circuit boards). In addition to the I^2C communications bus, there are global event trigger lines that are routed directly to every circuit board. These global trigger lines form the Event System, which allows high-speed triggering of pre-defined behavior through TTL without the overhead of USB or serial communications. The block diagram in figure 2 shows how master-daughter and event system communication is routed.

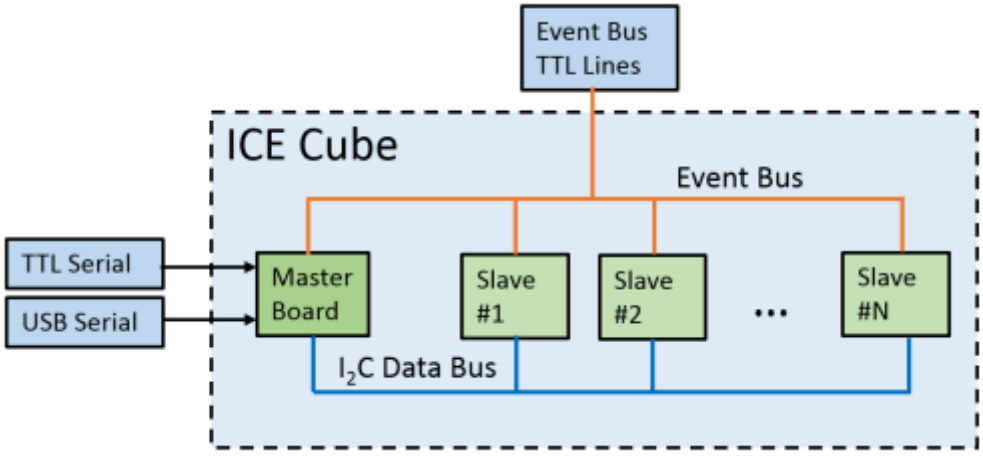


Fig. 2: Communication system block diagram.

Considerations for integrating the ICE Platform stack in an OEM situation are detailed in the remainder of this document. Important key points include deciding on the type and quantity of daughter modules to use and how that relates to the overall power budget for both the power supply and the maximum currents that can be routed through the power bus. The mechanics of mounting the circuit boards and designing a thermal management system must also be designed. Connections for communication and I/O from the circuit boards to the integrator's system are also detailed in the document.

Can't find what you are looking for? A forum has been established for Q&A and information dissemination. We invite you to join.

Power Requirements

Power Entry

Power needs to be supplied to the power bus headers on all ICE circuit boards. These headers and respective supply voltages are shown in figure 3. The ICE master controller board (ICE-MC1) takes a single power entry point and distributes power to these headers. The master controller board also provides fault protection, power sequencing, in-rush current protection, and over-current protection in addition to distributing power. It is highly recommended to only power the ICE board stack through an ICE master controller for these functions. If power is applied by the OEM integrator directly to the ICE power bus, the ICE power sequencing and protection requirements in this document must be strictly followed to avoid damaging connected ICE modules.

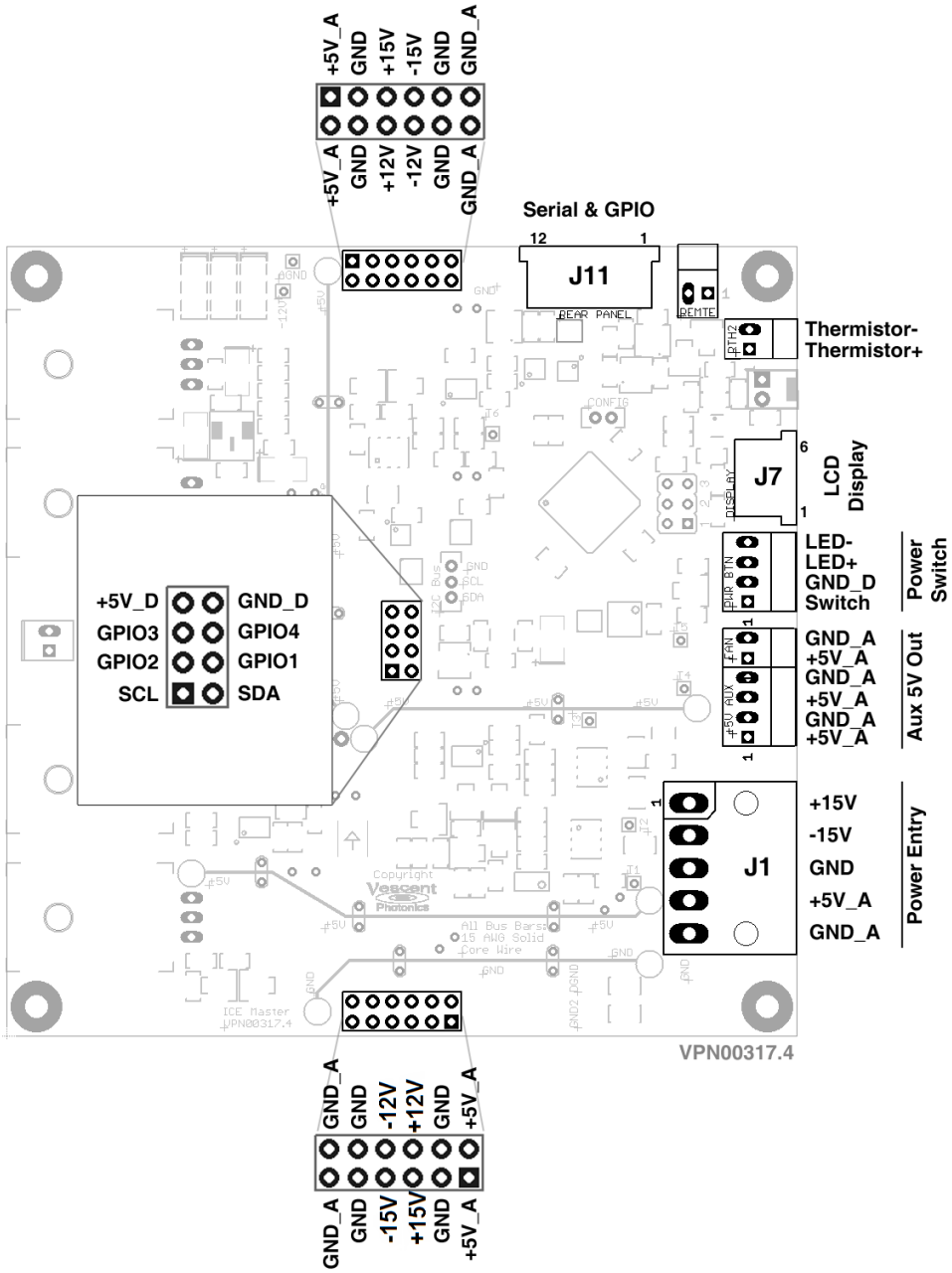


Fig. 3: ICE-MC1 Master and Control Board connector schematic (as viewed from component side).

Power Entry Through ICE Master Controller

Power is provided at J1 (Molex P/N: 0039303056). Pin definition shown in figure 3. The return current path for +5V_A is GND_A. This wiring connected to this return path should be capable of carrying the maximum current of the +5V_A line. Since the master controller handles all power sequencing requirements, the power connections for 5V_A, +15V, and -15V can be applied in any order so long as both ground connections have been established. The master controller will not turn on if any of the required voltages are not present or are out of range. These power entry inputs are also reverse-polarity protected. When the master controller enables power to the daughter boards via the power bus, power is in-rush current limited to less than 10A on the 5V_A line and 3A on the 15V lines.

The signals GND and GND_A are shorted together on the circuit board through a jumper, but this can be removed.

Power Entry Via Direct Power Bus Connection

Direct power connection to the power headers on ICE daughter modules is discouraged due to possible damage to modules if proper power sequencing is not followed.

Power can be provided directly to the internal power bus headers if no master controller is used in the system, but this is highly discouraged as the power requirements are much more strict in order to prevent damaging system components. There are three power bus connectors shown in figure 3 that utilize 0.1 inch double row board to board headers. The 6×2 headers (Samtec PN: ESQ-106-13-T-D) on either side of the pcb carry 5V_A, +15V, +12V, -12V, -15V power rails and GND_A and GND signal. Both of the headers must be powered by the same power rails and be connected to the same grounds. The signal name GND_A is the return current path for the 5V_A rail which provides high current to daughter modules which require it (such as the ICE-QT1). The 4×2 header (Samtec PN: ESQ-104-13-T-D) in the center of the pcb carries the digital communications bus and +5V_D power rail. The 5V_D power rail is designed to provide power to noisier digital components without contaminating the other analog power rails. This power rail can be “starred” off of the 5V_A line. All ground connections (GND, GND_A, GND_D) are intended to be starred at the power supply. The power sequence for turning on and off each voltage rail must be followed as described in the power sequencing section or damage will occur.

Power Draw by Module

The power supply capacity for the supply used to power the ICE stack must be sized appropriately to handle expected power draw for the modules selected. Current draw is listed in the specifications for each of the daughter modules. The typical values indicate the quiescent current draw, and the max values represent worst case power draw depending on the functionality of the board. For example, the ICE-QT1 quad temperature controller has a maximum expected current draw on the 5V_A rail that depends on the maximum current supplied to thermo-electric coolers (TEC's). The maxiumum current here depends on what the user sets the current limit to for each temperature controller section. The max spec given is based on the highest current limit being set for each section, and the power supply should be capable of supply that current unless those current limits are set lower. Another example are the ICE-CS1 and ICE-CP1 modules, both of which include a laser current controller. The current draw on the +15V depends on the laser current output, which has a maximum output current that can be used to determine total current draw. This is detailed in the specifications charts on the respective product pages for all these modules.

The ICE-MC1 master controller and ICE power bus have a maximum amount of current that can be routed. This is specified in the maximum power consumption specification on the ICE-MC1 product page. When choosing how many and which type of each daughter module a master controller can support, the expected current draw of all daughter modules must not exceed the maximum power consumption specification for the master controller. For example, the master controller and ICE power

bus can only distribute a maximum of 10 amps on the 5V_A rail. If three ICE-QT1 temperature controllers were chosen as daughter modules, and all the TEC current limits were left at maximum, the three modules could potentially draw 12 amps. This would exceed the capacity of the power bus and master controller. The master controller provide over-current protection, so it would shut down power to the daughter modules and enter a fault condition if 12 amps were attempted to be drawn from the 5V_A rail.



When choosing how many and which type of each daughter module a master controller can support, the expected current draw of all daughter modules must not exceed the maximum power consumption specification for the master controller.

Power Sequencing



Power sequencing is not required if using the ICE-MC1 master controller as it handles sequencing and startup commands automatically.

The ICE power bus that distributes power to all daughter modules must have each voltage rail properly sequenced when turning power on and off. The ICE-MC1 master controller automatically takes care of this power sequencing to protect daughter modules. If power is being applied directly to the power bus by the OEM integrator, the power sequencing outlined in this section must strictly be followed to prevent damage to the daughter modules. Between each step, an appropriate amount of settling-time should given for the previous power rail to settle (fully turn on or off) before proceeding to the next step. This is generally at least 100 milliseconds for most power supplies and voltage regulators. The I^2C broadcast commands are detailed in the communications section, but are included here to show the timing of when the commands should be sent. These commands are required to be sent for safe shutdown and proper operation of ICE daughter modules.



The I^2C System Ready and Shutdown commands are required to be sent for safe shutdown and proper operation of ICE daughter modules.



A delay of 100 ms (unless otherwise noted) is a generally sufficient time to wait between each power sequence step to allow the power supply to settle.

Power On Sequence

Step	Action
1	Enable 5V_D rail
2	Enable external 3.3V pull-up resistors on I^2C and GPIO[1)]
3	Enable +15V rail
4	Enable +12V rail
5	Enable -15V rail
6	Enable -12V rail
7	Enable 5V_A rail
8	Wait 2.5 seconds
9	Broadcast System Ready I^2C command[2)]
10	Broadcast Interlock Off I^2C command[3)]

Power Off Sequence

Step	Action
1	Broadcast Shutdown I^2C command[4)]
2	Wait 1 second
3	Disable 5V_A rail
4	Disable -12V rail
5	Disable -15V rail
6	Disable +12V rail
7	Disable +15V rail
8	Disable external 3.3V pull-up resistors on I^2C and GPIO[5)]
9	Disable 5V_D rail

Power Button

The ICE-MC1 master controller is designed to allow a push switch to be wired up to turn on and shutdown the ICE stack. There is a 4-pin Molex connector (Molex PN: 22-05-3041) which allows for connection to a “OFF-Mom” style (normally off, momentary on) push switch and power for an LED to indicate power state. The pin diagram is shown in figure 3, labeled as “Power Switch”. For reference, the pin definition is shown in table 1.

Pin	Name	Function
1	Switch	Connect to one terminal of push switch
2	GND_D	Connect to other terminal of push switch
3	LED+	Provides 5V to connect to positive terminal of LED
4	LED-	Connected to ground (GND_D) through 249Ω resistor and transistor

Tab. 1: Pin definitions for power switch connector

The momentary push switch should short to GND_D (provided on the connector) when activated. The master controller handles switch debouncing and will toggle the system power on and off with each press of the switch. For testing and toggling system power without an external switch connected, there is a SMD tactile switch located on the underside of the master controller circuit board that is wired in parallel to the external switch.

The default behavior of the master controller is to remain powered off (no power is being distributed to the daughter modules) when power is first applied to the board's power entry connector. Only after the power switch is pressed will the master board turn on and provide power to the daughter modules. The master controller will be completely powered off and will not respond to serial commands until the power switch is pressed. Note that this behavior can be changed at the factory.



The master controller will not turn on when power is applied to the power entry module. The power switch must be toggled once to turn on power. This behavior can be changed at the factory.



If no push switch is desired, the momentary switch can be replaced with a MOSFET controlled by another part of the OEM system.

Mechanics

Mounting

The ICE stack needs to be mounted to a grounded chassis. Each ICE circuit board has mounting holes located in each corner for 4-40 thread standoffs. Please see the PCB Mechanical Specifications page for measurements and technical drawings.



The mounting holes on each ICE circuit board are connected to system ground (GND).

The primary method for mounting ICE boards to is to create a board stack as shown in figure 4. The board stack is then affixed to a device chassis through the four 4-40 standoffs on either or both ends of the stack. The ICE boards use board-to-board headers to create its own internal backplane for power bussing and communications.

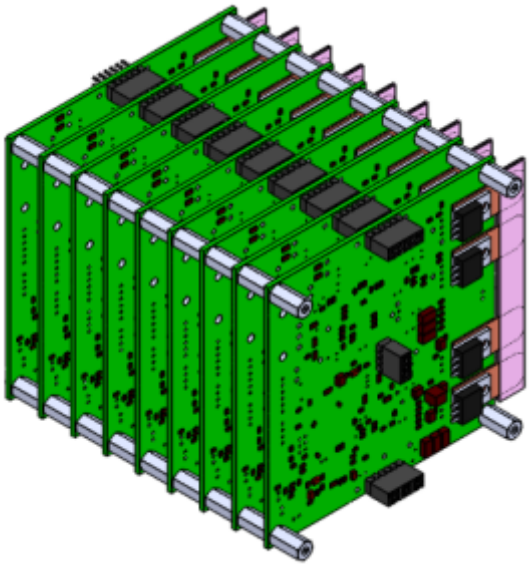


Fig. 4: ICE circuit boards in a stacked configuration

An alternative style of mounting is to attach each circuit board side by side in the same plane. In this case, no boards would be stacked on top of one another and a custom designed circuit board would have to be used as backplane. This backplane circuit board would distribute power and communications between the boards using the same 0.1 inch headers (see PCB Mechanical Specifications page for part numbers) used on each ICE board.

Thermal Management

Please see PCB Mechanical Specifications page for more details and technical drawings.

Each PCB exposes up to 4 copper tabs to conduct heat out from power dissipating components to an external heat sink. The copper tabs are not electrically isolated, so electrical isolation is **required** at the interface between the heatsink and copper tab. Failure to isolate these tabs will result in malfunction of the ICE module. For electrical isolation with good thermal conductivity, Sil-Pad can be used. Sil-Pad requires a certain amount of pressure to ensure good thermal conductivity, so a clamp mechanism should be applied to the copper tabs. The Sil-Pad is shown in pink in figure 5 and figure 6.

Further information on thermal management of the ICE boards, including CAD drawings of the heat sink clamp assembly, can be downloaded here.

Each copper heat sink tab must be electrically isolated from the heatsink and one another.

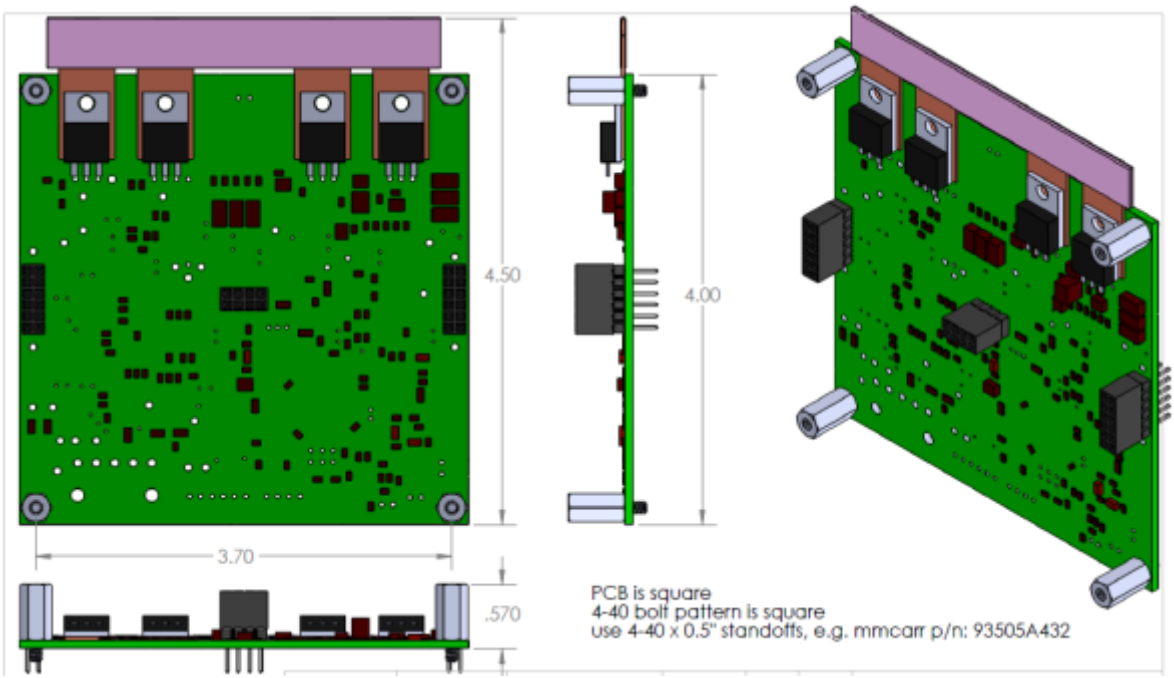


Fig. 5: Single PCB with Sil-Pad (shown in pink) wrapped around copper heatsink tabs.

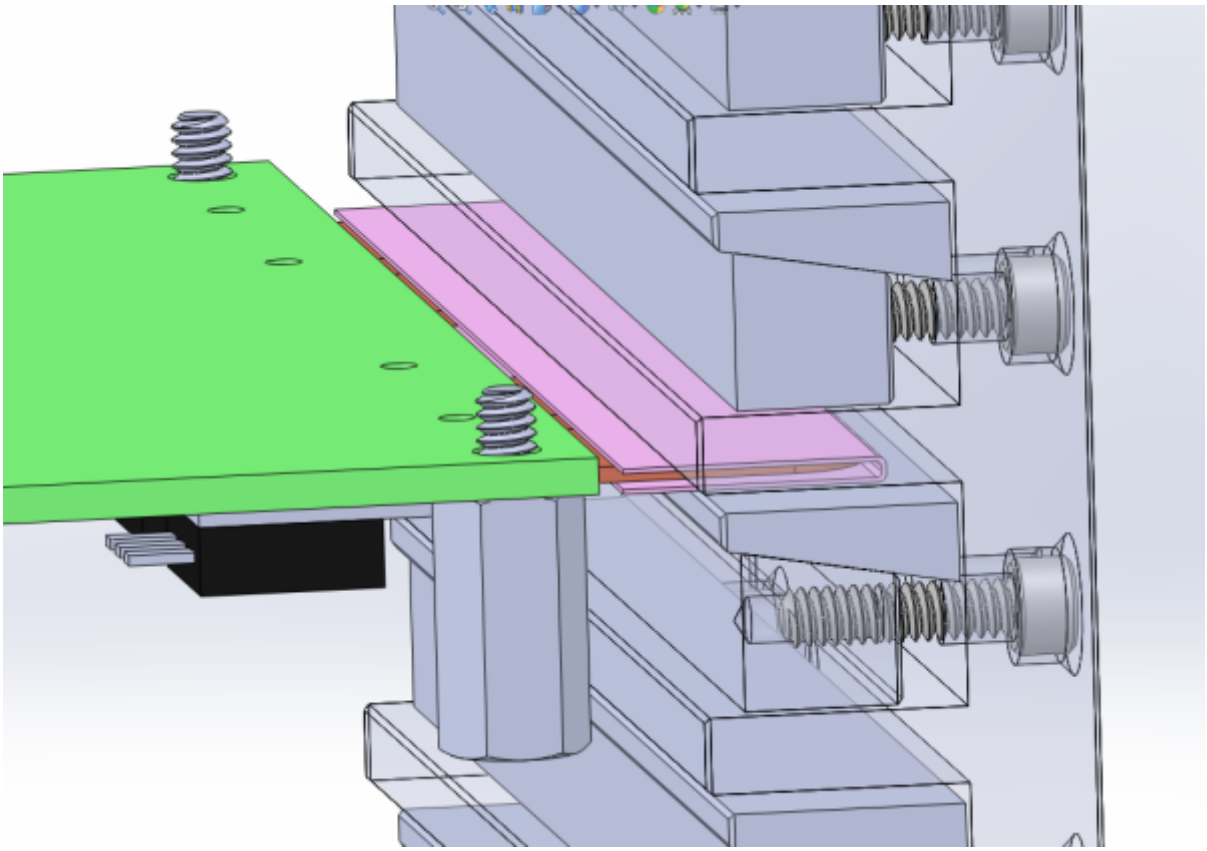


Fig. 6: Detail of a clamping mechanism used to conduct heat with electrical isolation.

Board Connections

Each ICE daughter module exposes analog interfaces on the side opposite to the copper heatsink tabs. Each module's circuit board may use a mixture of the connectors described in this section. Each connector and an associated part number shown below such that the OEM integrator my chose a suitable mating connector for their system. Consult the product pages for each ICE module to determine the type, position, and function of any connectors used. See the respective product pages

for each OEM board for a diagram of the positioning of any connectors.

For all ICE daughter modules, the circuit boards are designed such that all I/O connectors will be on a single side, and the copper heatsinking tabs will be on the opposite side. The master controller (ICE-MC1) also follows this convention, with the exception being the serial port flat flex connector.

Ultra-Miniature Coax Connector (UMCC)

The surface mount UMCC connectors (Molex PN: 0734120110) are used on the ICE-CS1 and ICE-CP1 for handling low-frequency analog signals (<8 GHz). A UMCC to UMCC cable or UMCC to SMA cable may be used to integrate these connectors with the OEM system.



Fig. 7: Surface mount UMCC connector. Molex PN: 0734120110



Fig. 8: UMCC to UMCC cable. TE Connectivity PN: 2015357-3



Fig. 9: UMCC to SMA Bulkhead cable. TE Connectivity PN 2032440-1

Flat Flex Connector (FFC)

These FFC connectors (FCI PN: SFW12R-1STE1LF) are used the ICE-QT1 to bring out the thermistor and TEC drive signals. Lower pin count ones are also used on the ICE-MC1 master controller for interfacing digital communications. Standard 1.00 mm pitch FFC jumper cables can be used to connect to an FFC connector on the other end. The ICE system uses right angle, 1.00 mm pitch, bottom contact FFC connectors.

Generally, the minimum bend radius for flat flex jumper cables is 2mm. The length of the stiffener behind the exposed contacts on the cable will determine how far out from the FFC pcb connector the first bend of the flat flex cable can occur. The clearance for this bend must be accounted for when designing an enclosure for the ICE boards. For example, with Molex brand flat flex cables, there needs to be a minimum 0.25 inch clearance from the front of the flat flex pcb connector to allow the cable to bend. Verify against the data sheet of the chosen flat flex jumper cable.



Fig. 10: Surface mount, 12-pin, 1.00 mm pitch, bottom contact FFC connector. FCI PN: SFW12R-1STE1LF



Fig. 11: FFC jumper cable, 12-pin, 1.00 mm pitch. Molex PN: 0210390269

SMA Connector

These board edge SMA connectors (Emerson PN: 142-0701-881)are used on the ICE-CP1 for handling high frequency RF signals (>8 GHz).



Fig. 12: SMA through-hole, right-angle connector. Emerson PN: 142-0701-881

Communications

This section details considerations for communicating with ICE modules in the system. For pin definitions and types of connectors for interfacing with the ICE stack, refer to the ICE-MC1 master controller product page.

I2C Addressing

The ICE board stack uses an I2C communication bus to control each board. I^2C is an addressable protocal, therefore each ICE daughter module needs to have a unique address set. Up to 8 daughter modules (not including the ICE-MC1 master controller) can be stacked together. Each ICE circuit board has a 3 position DIP switch (shown in figure 13) installed that allows the setting of each modules I^2C address (between 0-7). The selection of address is in binary with DIP position 1 corresponding to the least significant bit. Setting a bit “HIGH” is done by sliding the switch to the side marked with the word “ON”, which is shown highlighted in figure 14. An example address setting is shown in table 2. Valid I^2C addresses are from 0-7, and every ICE module must be set to have a unique address or communications bus collisions will occur.

DIP Position	Bit Value
1	1
2	1
3	0

Tab. 2: Example setting of DIP switch to I2C address "3".



Each ICE module must be set to have a unique address or communications bus collisions will occur.



Fig. 13: Photo of I2C address selection DIP switch.

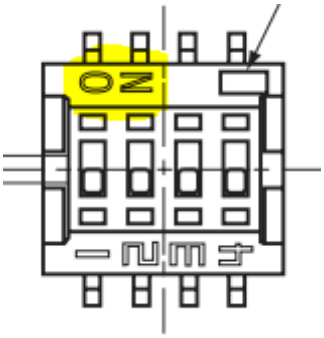


Fig. 14: The side which corresponds to ON or HIGH is highlighted in yellow.

Serial UART



The serial UART on the ICE-MC1 master controller runs at 3.3V signalling levels. Inputting 5V TTL signals will damage the circuit board. No voltage should be applied to the master controller USART lines when it is powered off or damage may occur (using series 1kΩ resistors on these lines is recommended).

The serial UART implemented on the ICE-MC1 master controller runs at 3.3V signalling levels. Inputting 5V TTL signals will damage the circuit board. When the master controller is in an off state (either from having been shutdown by the power switch or has just had power applied to its input but hasn't had the power switch pressed yet), no voltages should be applied to UART. Since the UART idles in a HIGH state usually, a serial device connected to a shutdown master controller could potentially feed 3.3V into an unpowered microcontroller and damage it. Two ways to prevent this are by taking advantage of using level-shifters or isolators if they are already needed in the system, or by simply using 1kΩ series resistors on all UART lines going into the master controller.

The FFC connector on the master controller also provides a 3.3V power rail to power an isolator or level-shifter. This power rail also indicates whether the master controller is powered or not and can be

used by a connected system to determine whether it is safe to allow signalling on the USART lines. If a level-shifter or isolator is to be used in the system, it is recommended to use this 3.3V rail to power the side connected to the master controller to prevent any signalling to go through to the master controller when it is unpowered.



If no level-shifting or isolation is desired, then it is recommended for the OEM integrator to use 1kΩ series resistors on all USART communication lines going into the master controller. These series resistors will protect the microcontroller from over-voltages up to 3.3V while it is unpowered.

USB to Serial Conversion

For ease of communication from a PC, it may be desirable to use a USART to USB converter. A commonly used IC to do this is an FTDI 232RL. This FTDI chip connects to the 3.3V UART interface and then creates a virtual COM port on the PC connected to it. Standard methods of interacting with serial ports may then be used for sending commands to the ICE-MC1 master controller. The FTDI chip has an onboard 3.3V regulator and can be configured to signal at 3.3V on the serial UART lines. In accordance with the UART protection recommendations given above, the 3.3V power rail provided from the master controller can be used to power the FTDI chip's UART signalling pins, thereby preventing any damage from occurring by signalling into an unpowered microcontroller on the master controller. If this technique isn't used, series resistors should be used on the UART lines.

Sometimes the PC communicating with the ICE modules may be located far away or on a different power circuit in the building. In this case, it may be desirable to isolate the power and ground of the PC (via the USB cable) by using an galvanic isolator. The easiest place to put this isolator is between the FTDI chip and UART of the master controller. The master controller's 3.3V rail can be used to power one side of the isolator and the USB 5V rail can be used to power the other. The ICE Platform enclosure uses an Analog Devices ADUM7441 to do this. An example implementation of this is shown in figure 15.

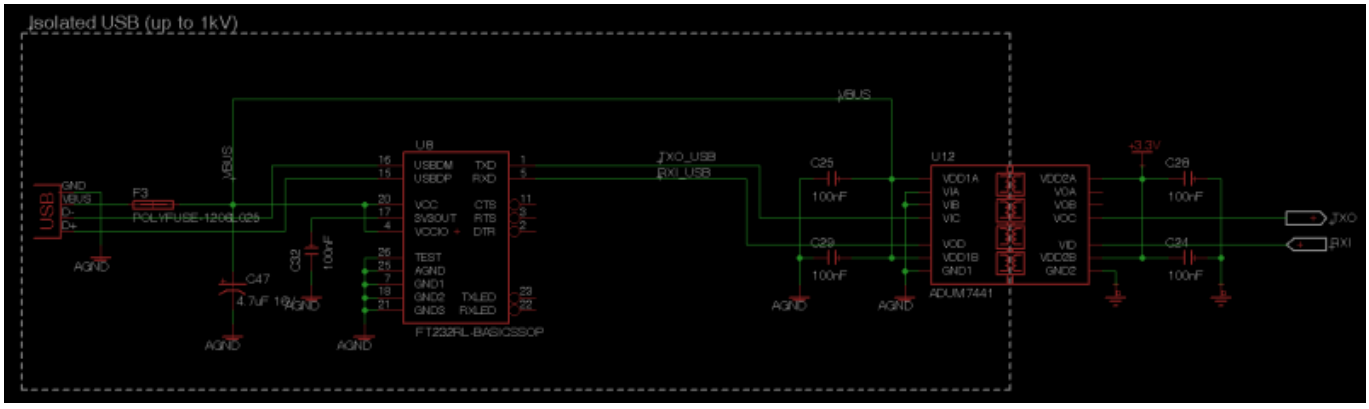


Fig. 15: Example implementation of USB isolation using ADUM7441

Power Command Sequence

When power up or shutting down the ICE modules, there are two I^2C commands that must be sent. The ICE-MC1 master controller automatically sends this commands and sequences the power rails, so sending this commands is not necessary if the ICE-MC1 is used.

At power on, once all voltage rails have been turned on and settled, the “System Ready” I^2C command should be sent to the stack. It is advisable to wait at least 2.5 seconds after the last power rail has been turned on to send this command. See the power sequencing section for timing details. The ID of this command is 7 and takes no arguments. To send the command, send an I^2C packet on one byte with the value of 0x07 to each ICE daughter module address (possible addresses are 0-7). In addition, the “Interlock” command should be sent to allow all modules that have a laser current controller to turn on. The interlock command has an ID of 12 and an argument of 1. To send the command, send an I^2C packet on two bytes with the value of [0x0C,0x01] to each ICE daughter module address (possible addresses are 0-7).

Before turning off any voltage rails for shutdown, the “System Shutdown” Read I^2C command should be sent to the stack. The ID of this command is 3 and takes no arguments. To send the command, send an I^2C packet on one byte with the value of 0x03 to each ICE daughter module address (possible addresses are 0-7). This packet should be sent at least 1 second before turning off any power rails to give time for all ICE daughter modules to prepare for a clean shutdown. Again, see the power sequencing section for timing details.



These raw I^2C bus commands do not apply if using the ICE-MC1 master controller.

Digital Communications Bus Header



Details in this section do not apply if using the ICE-MC1 master controller.

The communications bus goes through a 0.1 inch board-to-board header located in the center of each ICE circuit board. See the figure 3 for the pin definitions. If connecting directly to the ICE board stack without using an ICE-MC1 master controller, external pull-up resistors must be implemented by the OEM integrator on all the communication signals in this header (SDA, SCL, GPIO 1-4). The OEM integrator should use 1kΩ resistors pulled up to 3.3V on all these lines. The GPIO event bus lines are active low, but must float high when not in use. The SDA and SCL signals for the I^2C bus must always have pull up resistors no bigger than 1kΩ.

[1)](#) [5)](#)
These pullups are detailed later in the communications section
[2)](#) [3)](#) [4)](#)
This command is detailed in the communications section

From:
https://www.vescent.com/manuals/ - **Product Manuals**

Permanent link:
https://www.vescent.com/manuals/doku.php?id=ice:oem_integration&rev=1406061344

Last update: **2021/08/26 14:26**