SLICE-FPGA-II Manual

Model No. SLICE-FPGA-II
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Please read Limited Warranty and General Warnings and Cautions prior to operating the SLICE-FPGA-II.

Fig. 1: The SLICE-FPGA-II

Links

Click here for the Main Manuals Page.
Click here for the FFC-100 Quick Start Guide.
Click here for the FFC-100 API.

Description

The SLICE-FPGA-II is an FPGA-based locking instrument for use with a Fiber Frequency Comb such as the FFC-100. The included software allows for seamless locking of both the Carrier Envelope Offset and Optical frequencies.

Contents

The contents of the SLICE-FPGA-II box includes

- SLICE-FPGA-II
- USB memory stick with WinPython-64bit-3.6.1.0Qt5 and control software
- Power cord for your ship-to country
- An Ethernet cable for connecting your SLICE-FPGA-II to a computer.

Ensure that you received all of the materials. If you did not receive all of the materials, contact us at info@vescent.com

List of Warning Symbols

⚠️	Warning. Pay special attention to procedures and notes. If procedure is not followed carefully, damage to the SLICE-FPGA-II or devices connected to it may occur.
⚡	Potential for electrical shock hazard.

Absolute Maximum Ratings and Power Input

Note: All modules designed to be operated in a laboratory environment.

Parameter	Rating
Environmental Temperature	15°C<T<30°C
Environmental Humidity	<60%
Environmental Dew Points	<15°C
Maximum AC Line Input Current	2 A

Tab. 1: Absolute Maximum Ratings

Notice

⚠️	Do not block the airflow vents on the side of the chassis or the fan inputs & outputs on either the FFC-100 or the SLICE-FPGA-II.
	If this instrument is used in a manner not specified by the manufacturer in this manual or other relevant literature, protection provided by the instrument may be impaired.
	Successful implementation of the SLICE-FPGA-II depends critically on the design of the whole system: Frequency Comb, phase locking electronics, and any references to which the Frequency Comb is locked or *vice versa*.

Specifications

Inputs	
Parameter	**Value**
f_{OPT}	-30 ~ -15dBm
f_{CEO}	-30 ~ -15dBm
External Clock Input	0dBm [1]

Outputs	
Parameter	**Value**
Current Out	±10V
PZT Out	0-5V
Analog Slow Servo	±10V
10MHz Out	+3V TTL [2]

Tab. 2: Specifications of SLICE-FPGA-II Inputs and Outputs

Front Panel

Fig. 2: Front Panel of the SLICE-FPGA-II

1. f_{CEO} input (SMA)
2. f_{OPT} input (SMA)
3. Current output for modulating pump diode
4. PZT modulation output to modulate PZT
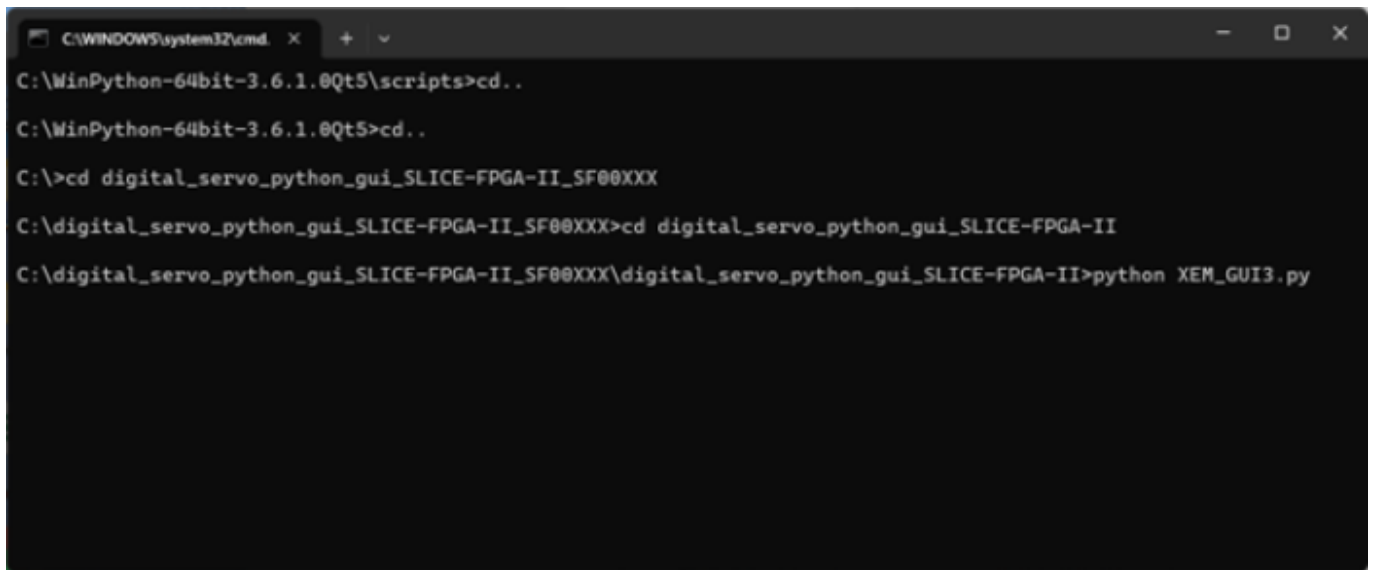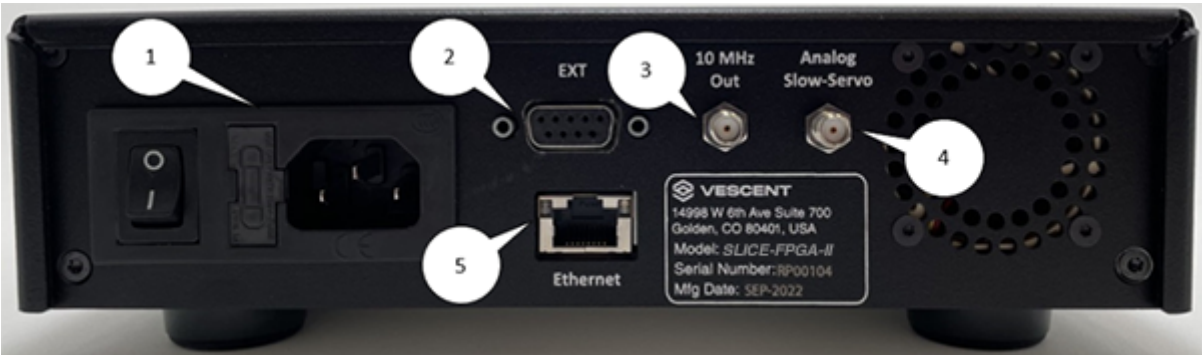5. External Clock Input. Use requires specifying input frequency in the settings menu.

Back Panel

Fig. 3: Back Panel of the SLICE-FPGA-II

1. AC power entry module and fuse
2. Extension port (unused)
3. Reference Clock signal (+3V 10MHz) for clocking external equipment
4. Analog Slow Servo control voltage (±10V)
5. Ethernet port for communication with a computer

Software Setup

- Install WinPython (WinPython-64bit-3.6.1.0Qt5) from the USB memory stick provided with the SLICE-FPGA-II in an easy to remember location. Do not use "WinPython-64bit-3.6.1.0Qt5" from the sourceforge.net or Github.net websites.
- Open the WinPython folder after installing WinPython, and launch the WinPython terminal within this folder.
- Navigate to the "digital_servo_python_SLICE-FPGA-II" folder and type "python XEM_GUI3.py" to start the GUI.

Fig. 4: Start-up Menu

- A start-up menu should appear (figure 5). Check that the software can recognize the ethernet connection to the module. If the module is recognized, the device name and IP address will appear next to "Connected FPGAs". If the device is not initially found, click "Broadcast discovery packet" to search for the device. Ensure "Push default values to Red Pitaya" is selected and press OK.
- If your computer does not see the SLICE-FPGA-II in the start up screen, consult the troubleshooting guide for additional help.
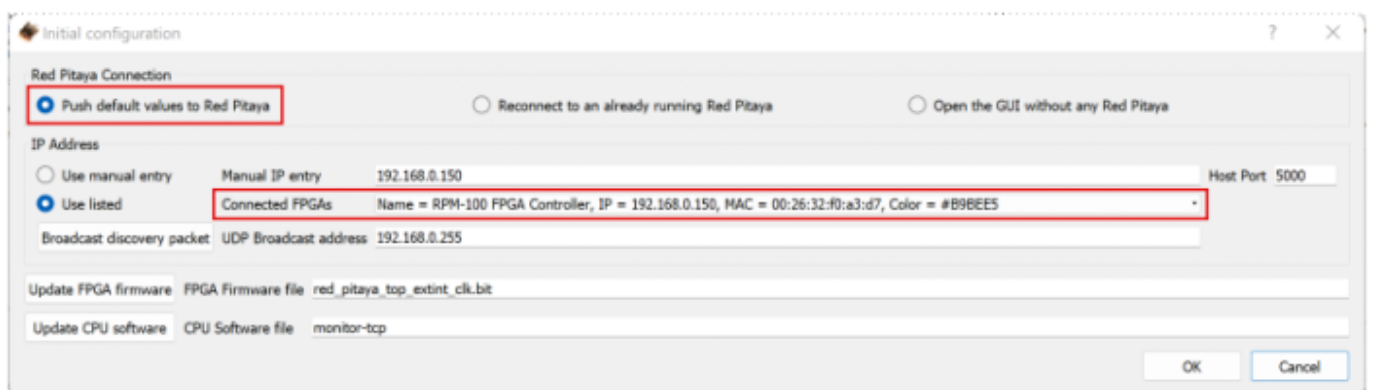

Fig. 5: Start-up Menu

FPGA Control

The SLICE-FPGA-II FPGA Controller can be used to phase lock f_{CEO} to a reference and f_{OPT} to a reference laser such as the Rio Planex. The SLICE-FPGA-II should be connected to a Vescent frequency comb (FFC or Comb Module) as shown below (figure 7).
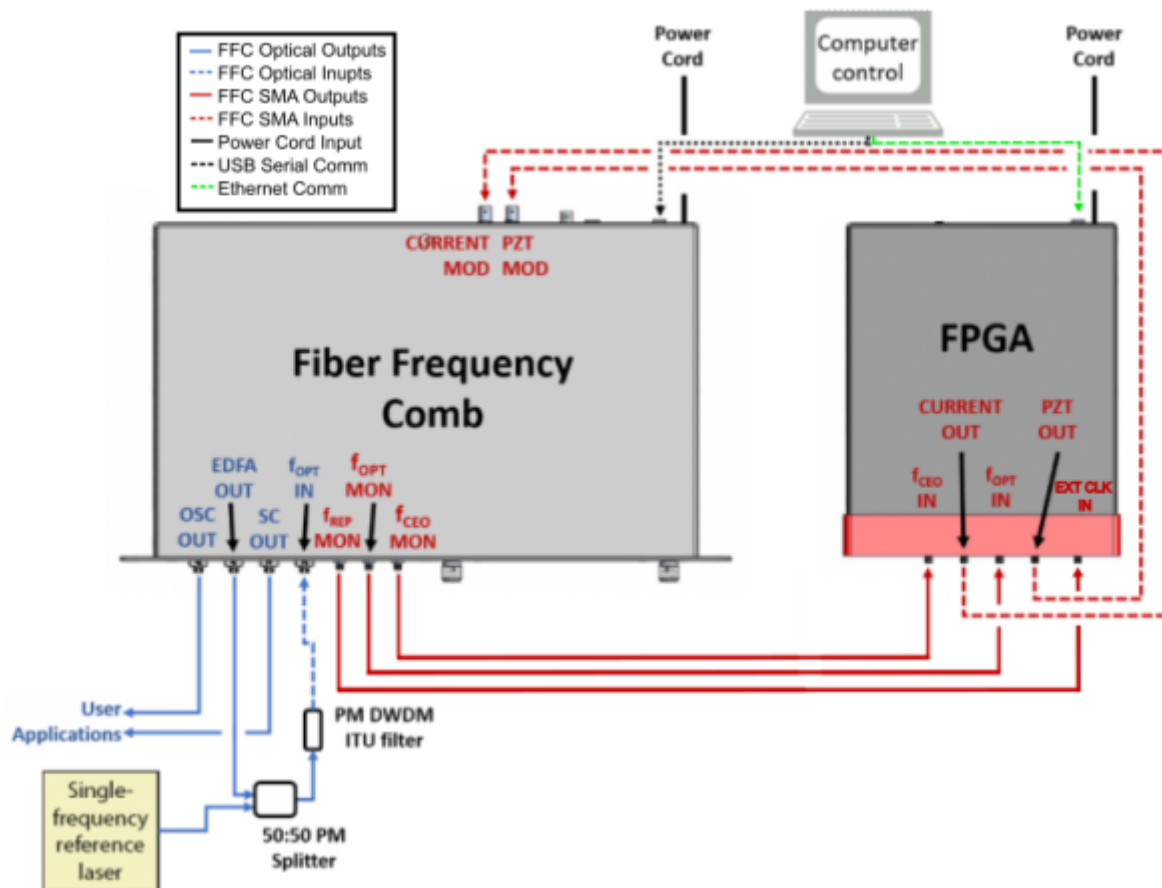

Fig. 7: System Level Diagram of the SLICE-FPGA-II Connected to an FFC-100

Locking f_{opt} requires a reference CW laser and heterodyne setup (such as a 50:50 beam splitter and DWDM filter). The stability of the lock will depend on the reference laser used. All Vescent performance data is collected with a Rio Planex laser.

External Clock

The external clock input (#5 on the Front Panel Diagram) allows the FPGA to be clocked with an external source, e.g. fREP from the FFC, or another system's master clock. Navigate to the "Settings" tab and select the appropriate clock signal to be used (figure 8). Enter the incoming clock's frequency (in Hz) into the "Target ExtClk Freq" box, press enter, and then press the "External clock" button above
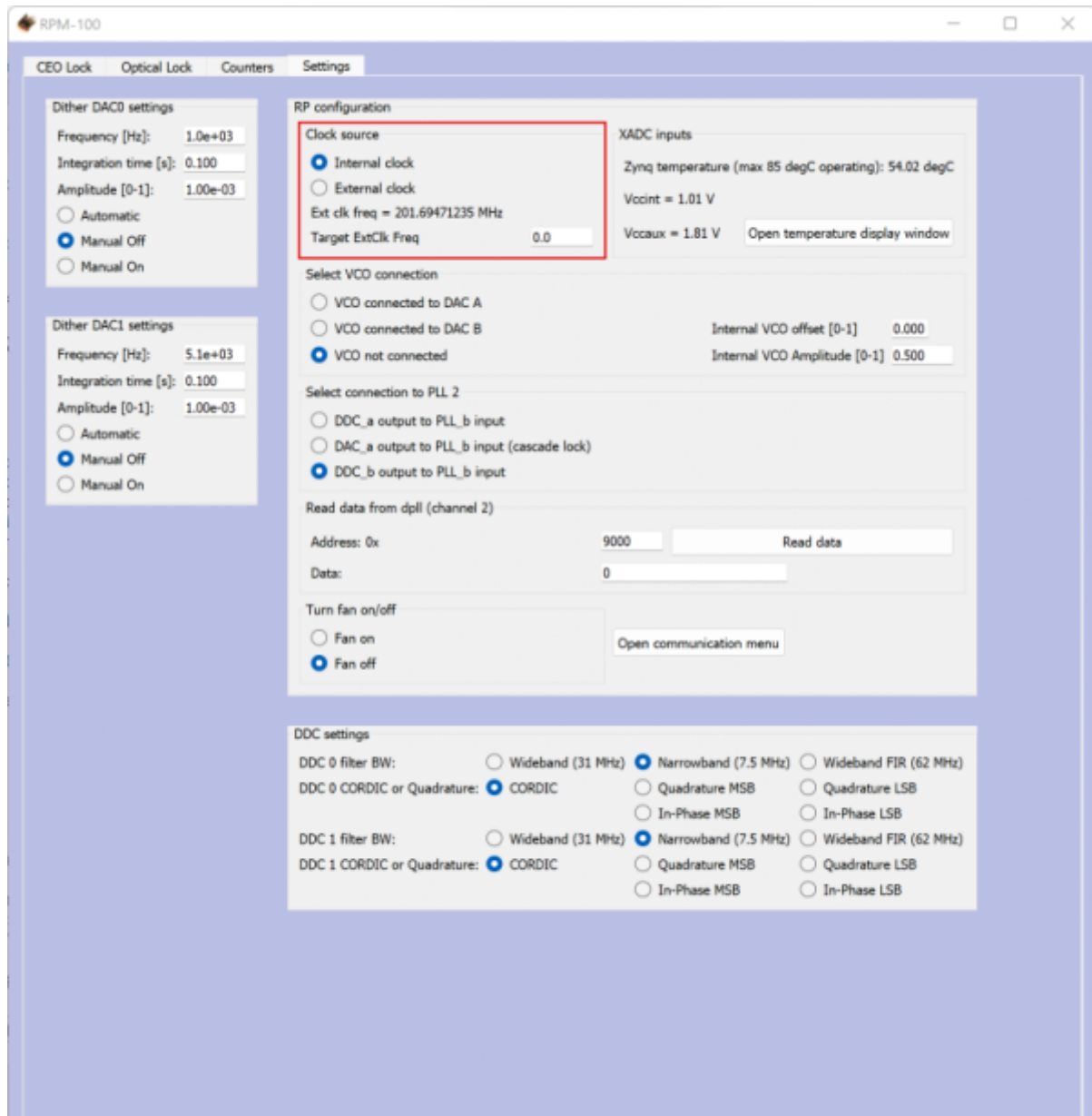
Fig. 8: Settings Tab

The SLICE-FPGA-II accepts a variety of discrete clock signal frequencies (15, 20, 25, 30, 40, 50, 75, 100, 125, 150, 200 and 250 MHz). Due to limitations of the internal dividers of the FPGA, certain external clock frequencies will result in an inaccurate absolute frequency reference. If a clock frequency other than those provided is required, please contact Vescent staff to discuss your application.

Locking ƒ(CEO)

1. Navigate to the "CEO Lock" tab and enable the "Auto-refresh" button in the top left of the window. Set your desired RF lock frequency of the Fceo beatnote in the "Reference Frequency [Hz]" input. Adjust the "Offset DAC 0" slider near the top left by clicking and dragging the slider until the Beatnote is roughly centered in the red filter trace (figure 9). It is also possible to adjust the FFC-100 oscillator current on its front panel to make this adjustment.
2. Note: If parts of the FPGA GUI window are cutoff, shift the window out of full screen and press the maximize window button.
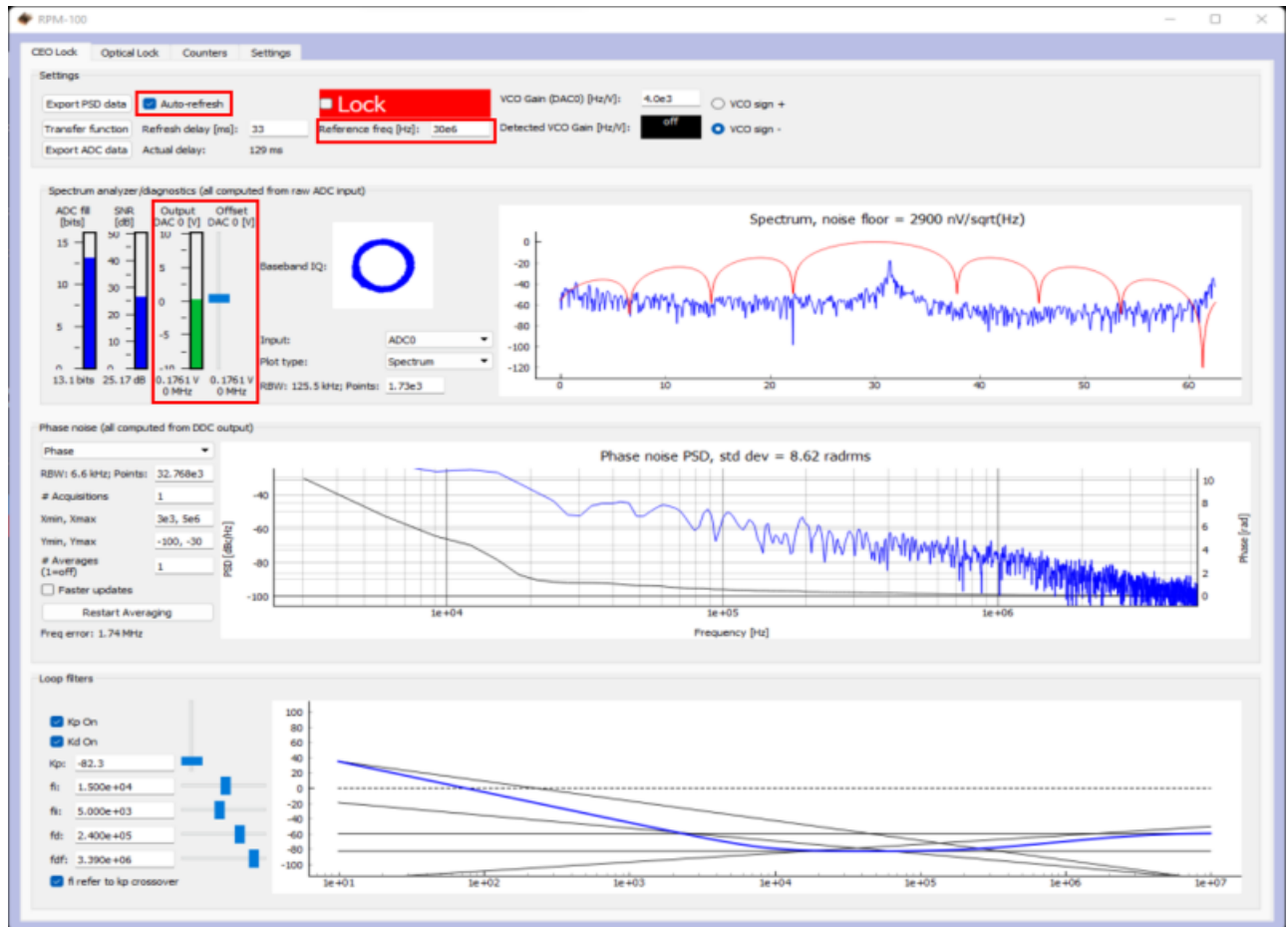
Fig. 9: Centering ƒ(CEO) on reference frequency (Baseband IQ optimization)

3. Press the "Lock" button (figure 10, top middle). If the system doesn't lock, change the VCO sign to the opposite polarity (top right) and try again. A warning may occur if the selected VCO sign is incorrect. If the system still won't lock, try lowering the K_p value (bottom left).

Fig. 10: Locking ƒ(CEO)

4. If the Beatnote is properly locked, the integrated phase noise value listed in the center of the window should be close to the value listed in your devices CoC.

Locking ƒ(opt)

1. Ensure that your laser reference source is properly mixed with the "EDFA Out" optical port of the frequency comb as described in the devices CoC and is input back into the device via the "ƒ$_{opt}$" input port at a power level of <1.5 mW.
2. Navigate to the "Optical Lock" window and enable the "Auto-refresh" button in the top left of the window. Set your desired RF lock frequency of the ƒ$_{opt}$ beatnote in the "Reference Frequency [Hz]" input. Adjust the "Offset DAC 1" slider near the top left by clicking and dragging the slider until the Beatnote is roughly centered in the red filter trace (figure 11).
3. Note: If parts of the GUI window are cutoff, shift the window out of full screen and press the maximize window button.

Fig. 11: Centerig ƒ(opt) on reference frequency (Baseband IQ optimization)

4. Press the "Lock" button (figure 12, top middle). If the system doesn't lock, change the VCO sign to the opposite polarity (top right) and try again. A warning may occur if the selected VCO sign is incorrect. If the system still won't lock, try lowering the K$_p$ value (bottom center).
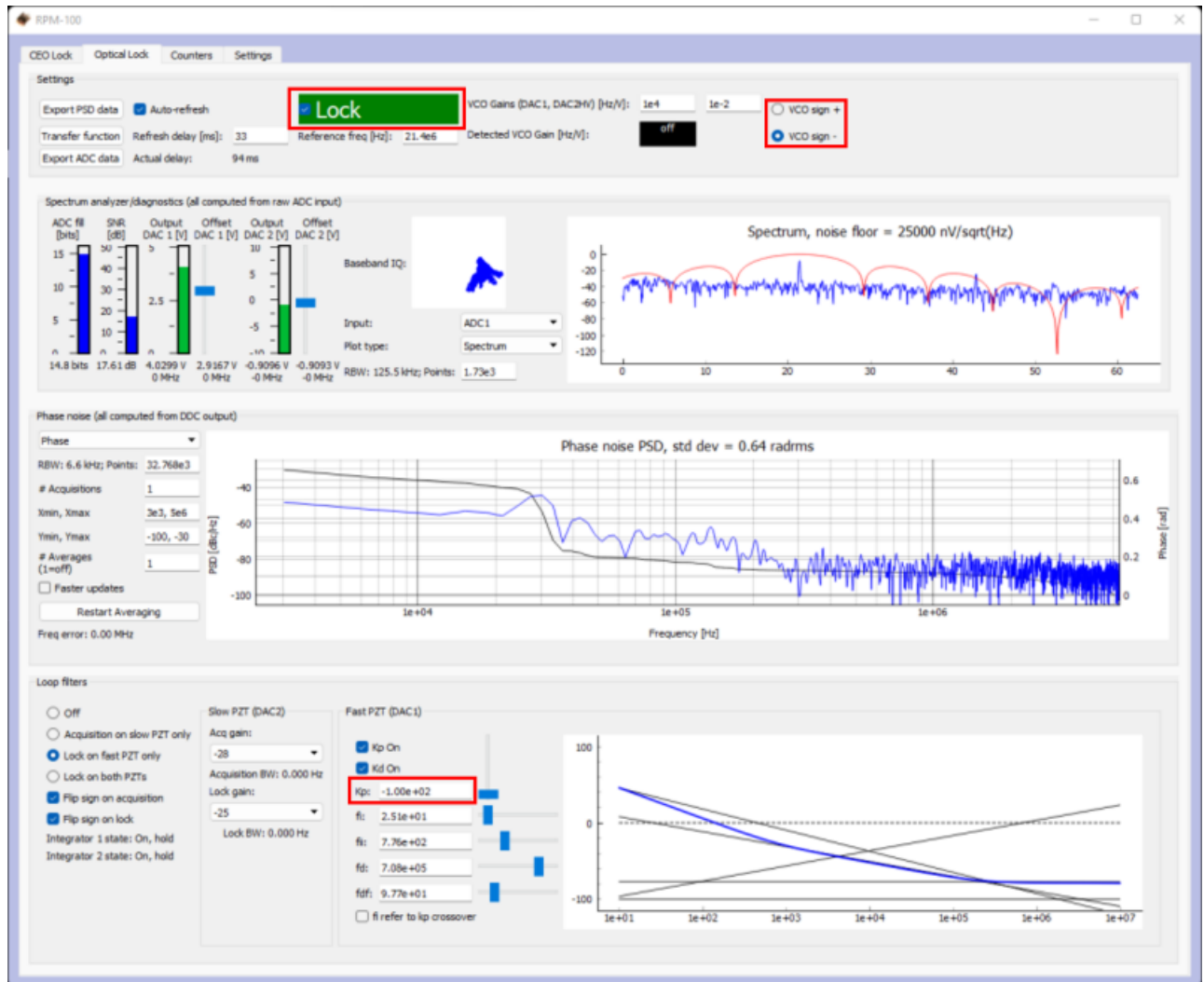
Fig. 12: Locking ƒ(opt)

5. If the Beatnote is properly locked, the integrated phase noise value listed in the center of the window should be close to the value listed in your devices CoC.

6. Adjust PID settings (bottom of figure 10 and figure 12) as needed to lower the integrated phase noise of each parameter (f_{CEO} and f_{opt}). The default settings provided in the software are tuned for your specific device but tweaking the values can often improve performance based on the noise characteristics of your environment.

Troubleshooting

Overview

In many cases, all that is necessary to get up-and-running with the SLICE-FPGA-II is to install the correct WinPython distribution, and run the provided GUI software using the WinPython terminal. If you are unable to connect the GUI to the SLICE-FPGA-II, follow the below instructions to eliminate possible causes of failure.

## Ethernet Controller IP Configuration

Whatever ethernet port you use to control the SLICE-FPGA-II, it is necessary that your computer

identifies itself on this Ethernet port with a fixed IP address in the **192.168.0.x subnet**. Sometimes a computer's default settings do not fit this requirement. From the Windows Control Panel, click through: Network and Internet –> Network and Sharing Center –> Change adapter settings

You will see a number of network adapters listed. You should see one of the network adapters change state when you connect the powered-on SLICE-FPGA-II to your PC via the ethernet cable, as shown below:
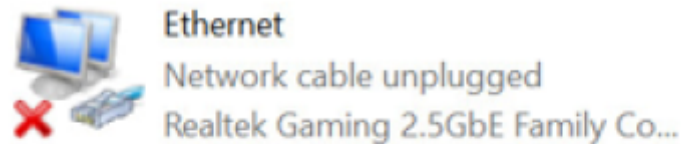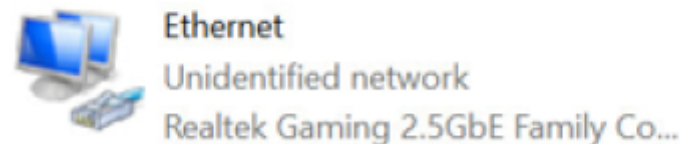
Watch for this change to identify the correct network adapter.

- Right-click on the adapter, and click **Properties**.
- From the screen that appears, click on "Internet Protocol Version 4 (TCP/IPv4)" and then click Properties.
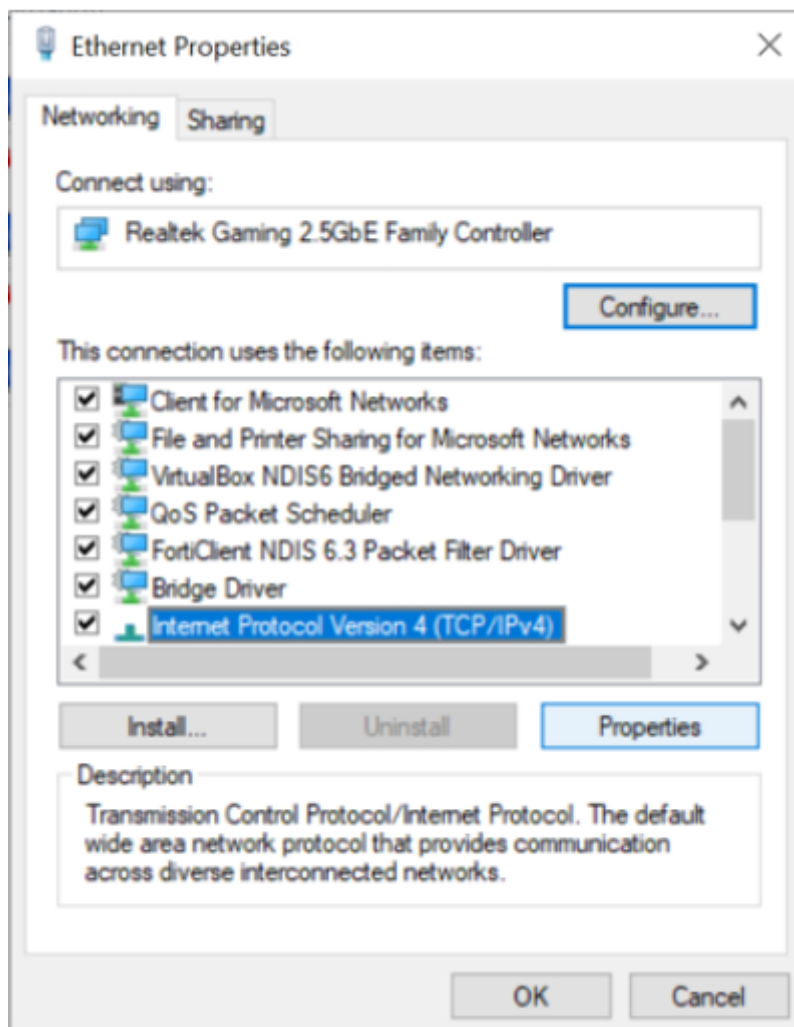
Fig. 13: The Adapter Properties screen, with the IPv4 Settings highlighted

- In the IPv4 Properties Page, select the bubble next to "Use the following IP address:", and fill in the IP Address to be **192.168.0.xxx**, where **xxx** is an integer from 0 to 255, and not **150**, as that is the address used by the SLICE-FPGA-II. In this example, we used 196.

Fig. 14: The IPv4 Properties page, with the IP Address and Subnet Mask filled in.

The Subnet Mask will default to 255.255.255.0, which is fine.

NOTE: If you use this same Ethernet port to connect to another network, these configuration changes could result in connectivity problems with that network. If this poses a problem for you, consider buying a USB-to-Ethernet adapter, and configuring just that adapter for use with the SLICE-FPGA-II.

Windows Firewall Rules

If you continue to have trouble connecting to the SLICE-FPGA-II, it's possible that your firewall settings are blocking communications with the device. From the Windows Control Panel, click on System and Security –> Windows Defender Firewall –> Advanced Settings to open up the **Windows Defender Firewall with Advanced Security** manager application. In the left panel of the program, click "Inbound Rules." Then, in the right-hand panel of the program, click "New Rule…" Use the "New Inbound Rule Wizard" to create a new rule to the following specifications:

- Rule Type: **Program**
- Program: **[WINPYTHON INSTALL DIRECTORY]\WinPython-64bit-3.6.1.0Qt5\python-3.6.1.amd64\python.exe**
- Action: **Allow the connection**
- Profile: **Domain, Private, and Public**
- Name: **Red Pitaya WinPython** (or another name of your choice)

In the left-hand panel, click "Outbound Rules", and then click "New Rule…". Repeat the above Rule

creation steps to create a rule that allows outgoing packets from the WinPython directory's "python.exe" file. Finally, ensure that the aforementioned python.exe file is not being restricted by any other firewall rules.

[1)]

Do not exceed +10dBm for the protection of the device

[2)]

at 10MHz

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