SLICE-FPGA-II Manual

Fig. 1: The SLICE-FPGA-II

Model No. SLICE-FPGA-II
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Please read Limited Warranty and General Warnings and Cautions prior to operating the SLICE-FPGA-II.

Links

Click here for the Main Manuals Page.
Click here for the FFC-100 Quick Start Guide.
Click here for the FFC-100 Fiber Frequency Comb Manual Click here for the FFC-100 API.
Click here for the latest version of WinPython

Description

The SLICE-FPGA-II is an FPGA based locking instrument for use with the FFC-100. Using the included software, the Carrier Envelope Offset and Optical frequencies of the FFC-100 can be locked with ease!

List of Warning Symbols

	Warning. Pay special attention to procedures and notes. If procedure is not followed carefully, damage to the FFC-100 or devices connected to it may occur.
	Potential for electrical shock hazard.

Absolute Maximum Ratings and Power Input

Note: All modules designed to be operated in a laboratory environment.

Parameter	Rating
Environmental Temperature	>15°C and <30°C
Environmental Humidity	<60%
Environmental Dew Points	<15°C
Maximum AC Line Input Current	2 A

Tab. 1: Absolute Maximum Ratings

Notice

	Do not block the airflow vents on the side of the chassis or the fan inputs & outputs on either the FFC-100 or the SLICE-FPGA.
	If this instrument is used in a manner not specified by the manufacturer in this manual or other relevant literature, protection provided by the instrument may be impaired.
	Successful implementation of the SLICE-FPGA-II depends critically on the design of the whole system: FFC-100, phase locking electronics, and any references to which the FFC-100 is locked or *vice versa*.

Specifications

Inputs	
Parameter	**Value**
f_{OPT}	-30 ~ 10dBm
f_{CEO}	-30 ~ 10dBm
External Clock Input	0dBm [1)]

Outputs	
Parameter	**Value**
Current Out	±10V
PZT Out	0V-5V
Analog Slow Servo	±10V
10MHz Out	+3V TTL [2)]

Tab. 2: Specifications of SLICE-FPGA-II Inputs and Outputs

Front Panel

Fig. 2: Front Panel of the SLICE-FPGA-II

1. f_{CEO} input signal SMA
2. f_{OPT} input signal SMA
3. Current output for modulating pump diode on the FFC-100
4. PZT modulation output
5. Output for feeding an external reference clock, which can improve 10MHz timing on onboard oscillator. Use requires specifying input frequency in the settings menu.

Back Panel

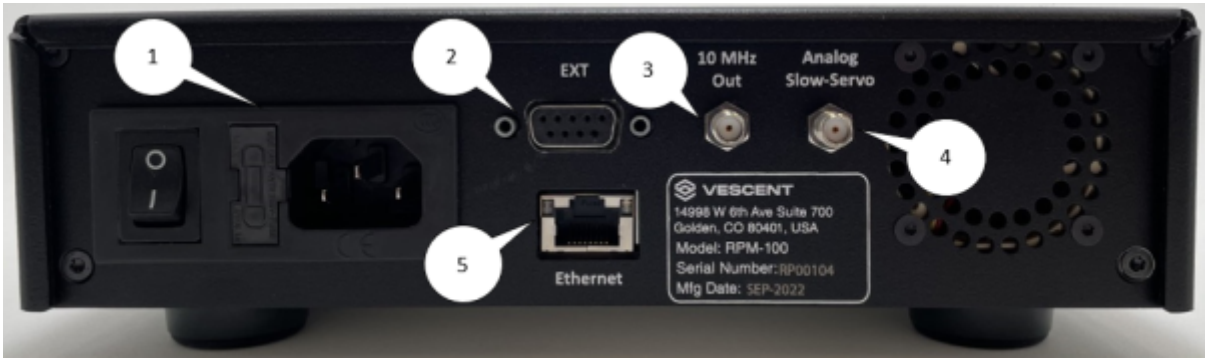


Fig. 3: Back Panel of the SLICE-FPGA-II

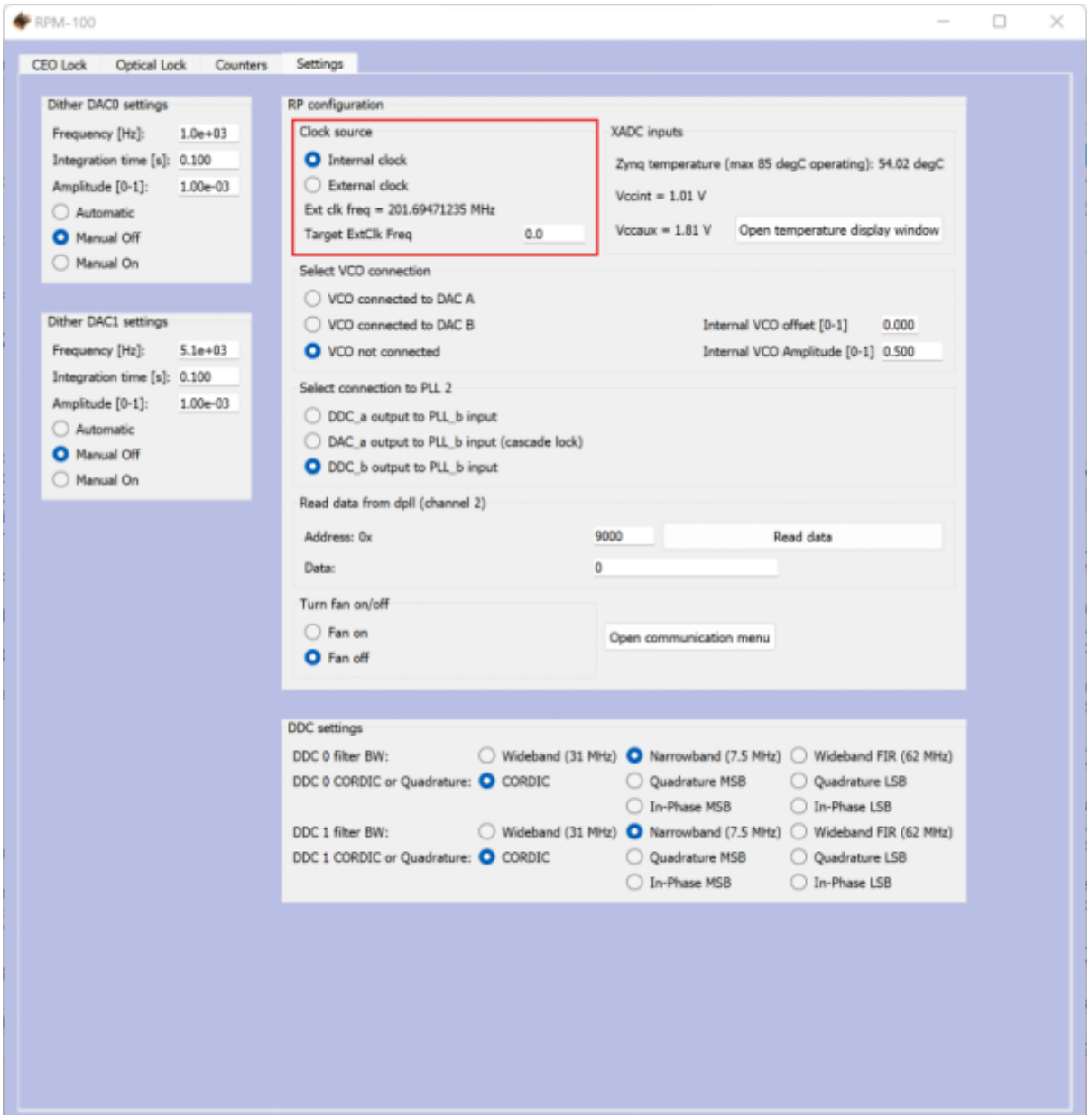
1. AC power entry module and fuse
2. Currently Unused Extension port
3. Reference Clock signal (+3V 10MHz) for clocking external equipment
4. Analog Slow Servo control voltage (±10V)

5. Ethernet port for communication with a computer

Software Setup

- Open the “WinPython-64bit-3.6.1.0Qt5” folder after installing WinPython, and launch the Spyder application within this folder.
- Open the “digital_servo_python_gui_RPM100” folder and locate the GUI control file named “XEM_GUI3.py”.
- Drag and drop the file into Spyder, and run the script to launch the GUI.
- A start-up menu should appear (figure ??). Check that the software can recognize the ethernet connection to the module. If the module is recognized, the device name and IP address will appear next to “Connected FPGAs”. If the device is not initially found, click “Broadcast discovery packet” to search for the device. Ensure “Push default values to Red Pitaya” is selected and press OK.

- Navigate to the “Settings” tab and select the appropriate clock signal to be used. If using an external clock, type the frequency (in Hz) of your reference signal.



FPGA Control

The SLICE-FPGA-II FPGA Controller can be used to phase lock f_{CEO} to a reference and f_{OPT} to a reference laser such as the Rio Planex. If you have not already done so, install WinPython for controlling the SLICE-FPGA-II.

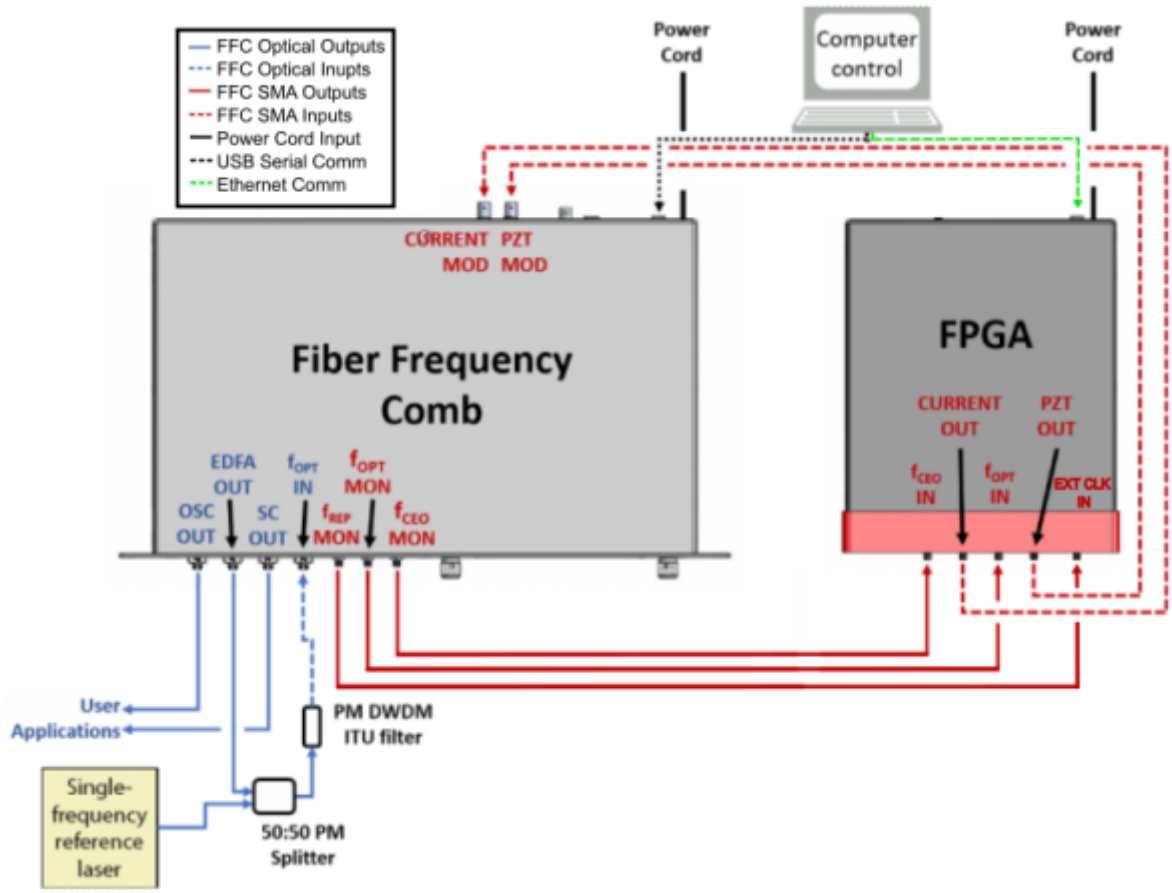


Fig. 4: System Level Diagram of the SLICE-FPGA-II Connected to an FFC-100

Locking f_{opt} requires a reference CW laser and heterodyne setup (such as a 50:50 beam splitter and DWDM filter). The stability of the lock will depend on the reference laser used. All performance data is collected with a Rio Planex laser.

Locking ƒ(CEO)

1. Navigate to the “CEO Lock” tab and adjust the “Offset DAC 0” slider near the top left by clicking and dragging the slider until the the data in the Baseband IQ plot is circular and the beat note is visibly centered under the middle red filter arch (figure 5). It is also possible to adjust the FFC-100 oscillator current on its front panel to make this adjustment.

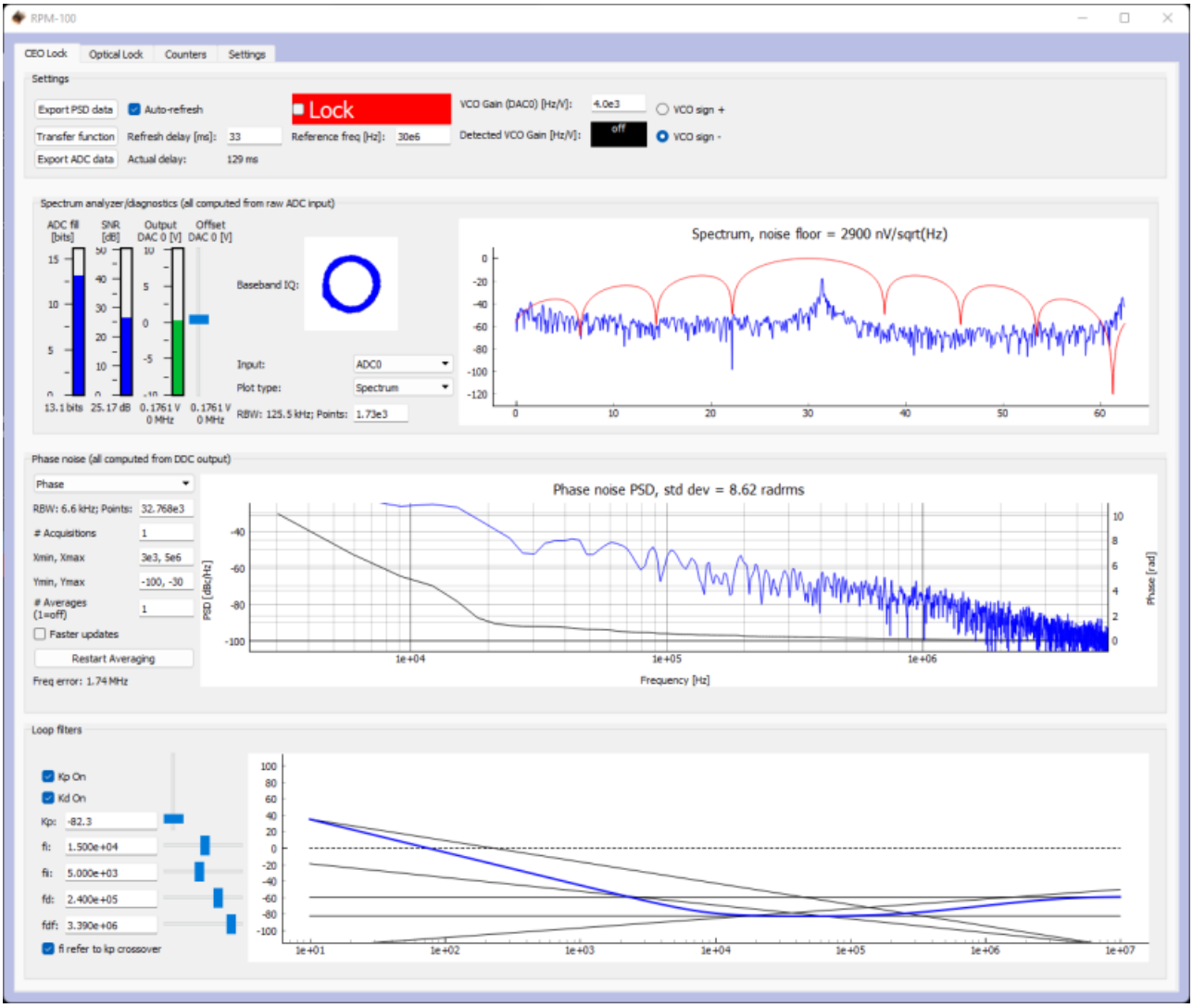


Fig. 5: Centering ƒ(CEO) on reference frequency (Baseband IQ optimization)

2. Press the “Lock” button (figure 6, top middle). If the system doesn’t lock, change the VCO sign to the opposite polarity (top right) and try again. If the system still won't lock, try lowering the K_p value (bottom left).

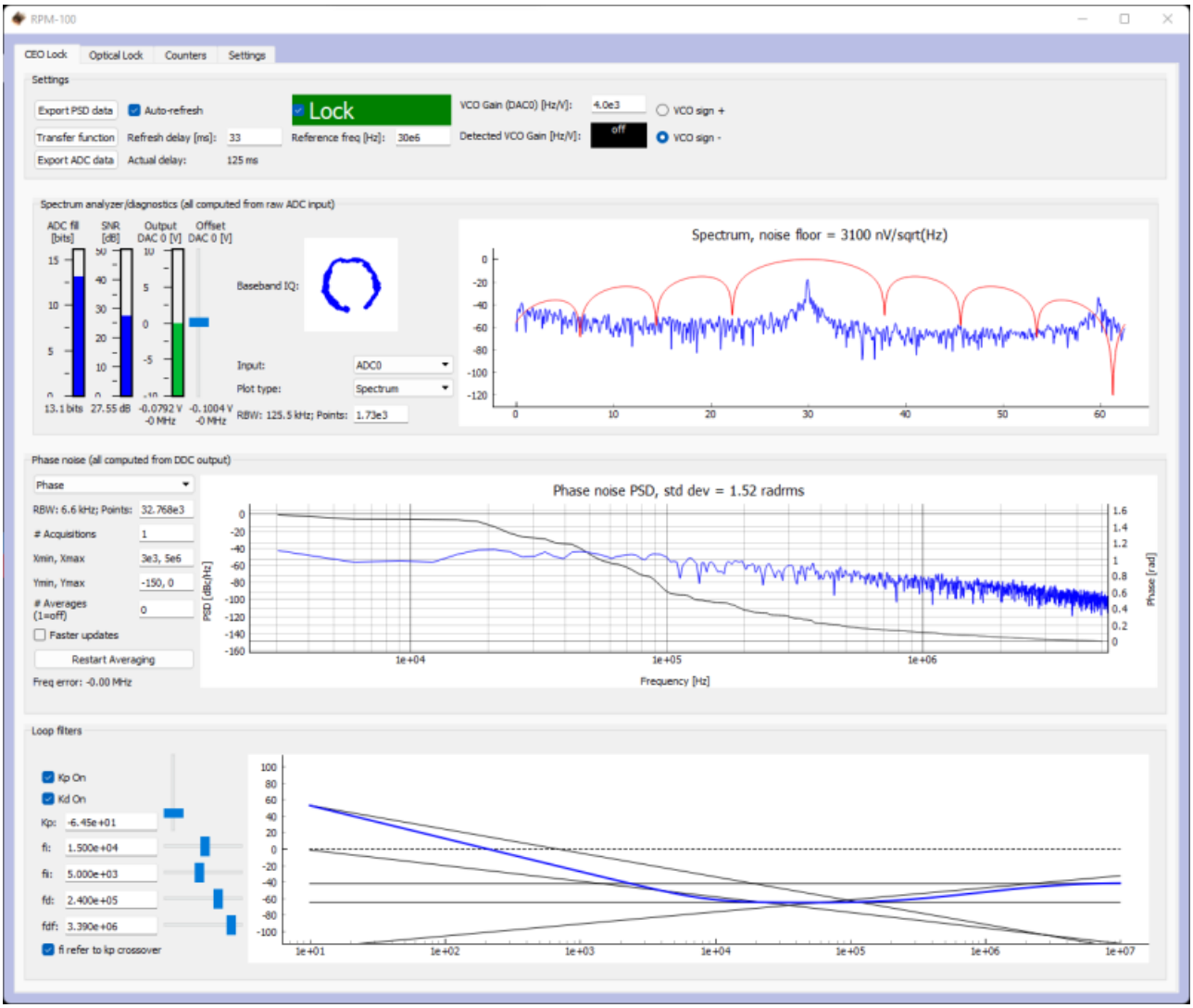


Fig. 6: Locking ƒ(CEO)

Locking ƒ(opt)

1. Navigate to the “Optical Lock” window. Center the beat note near the reference frequency: adjust the “Offset DAC 1” slider (or your reference laser frequency) until you see a circular Baseband IQ diagram (figure 7).

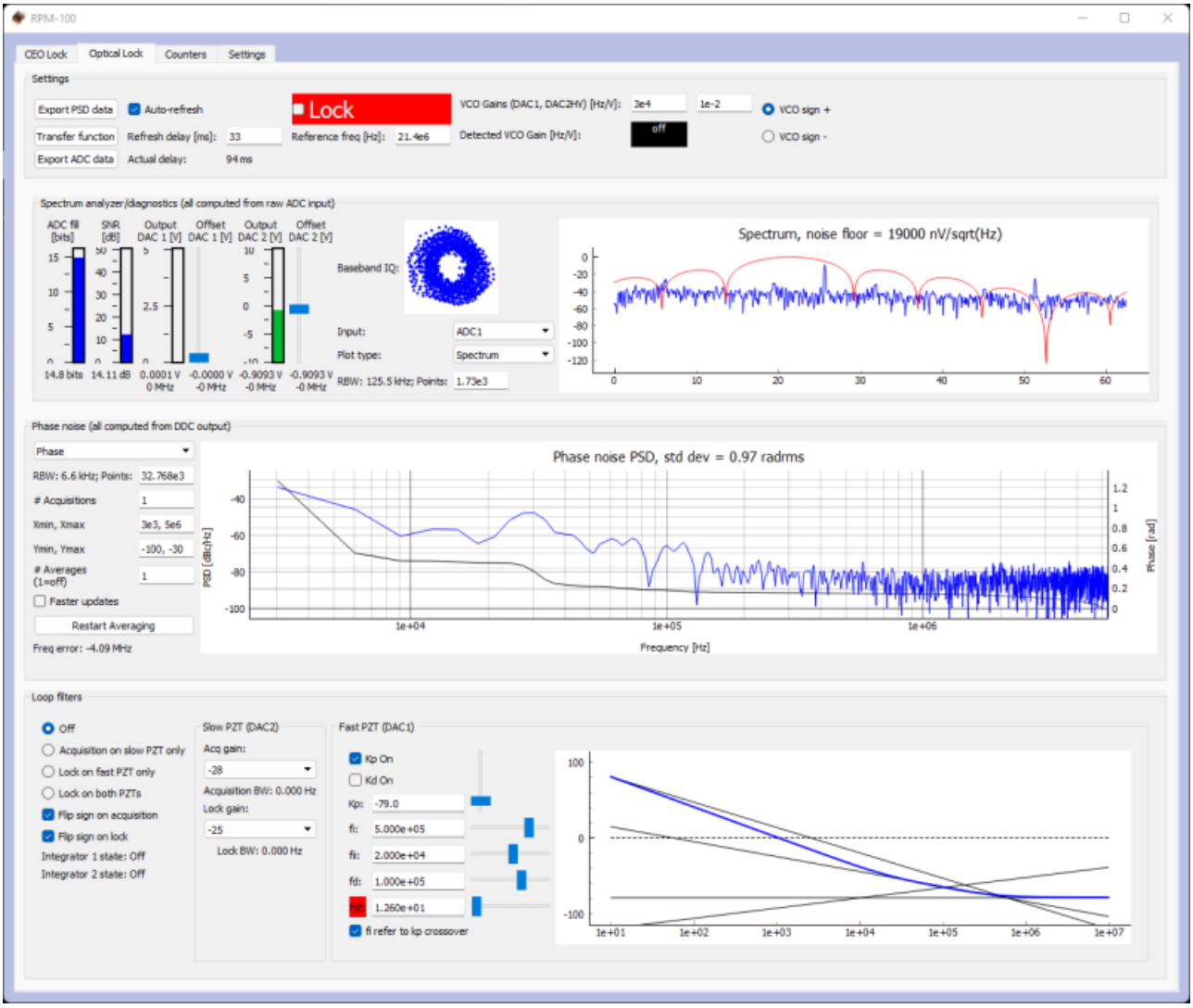


Fig. 7: Centerig ƒ(opt) on reference frequency (Baseband IQ optimization)

2. Press the “Lock” button (figure 8). If f_{opt} doesn’t lock, change the VCO sign to the opposite polarity and try again. If the system continues to not lock, lower the K_p value.

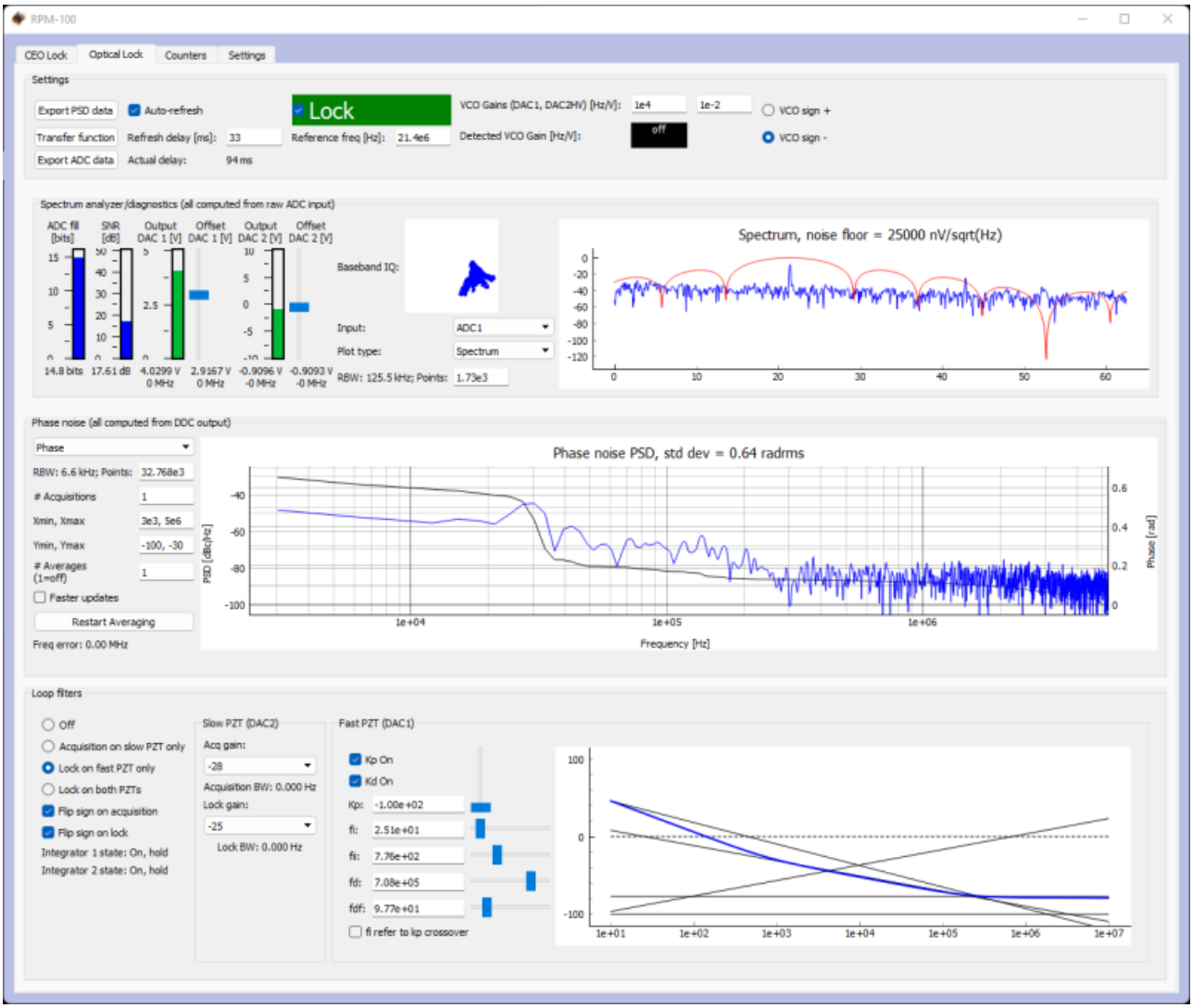


Fig. 8: Locking ƒ(opt)

3. Adjust PID settings (bottom middle of figure 8) accordingly to lower the integrated phase noise of each parameter (f_{CEO} and f_{opt}). The default settings provided in the software are a good place to start but tweaking the values can often improve performance.

External Clock

The external clock input (#5 on the Front Panel Diagram) is used to feed an external reference clock, which can be used to clock the SLICE-FPGA-IIs ADCs and generate the 10MHz reference signal which is normally generated with the internal oscillator. For example, the SLICE-FPGA-II can be clocked with an external reference, or the f_{REP} signal from the FFC-100. To use this feature, it is necessary to first specify the input frequency in the settings menu of the software provided with the SLICE-FPGA-II, under the “Target ExtClk Freq” box. Pressing ENTER after giving a value will apply the new clock settings.

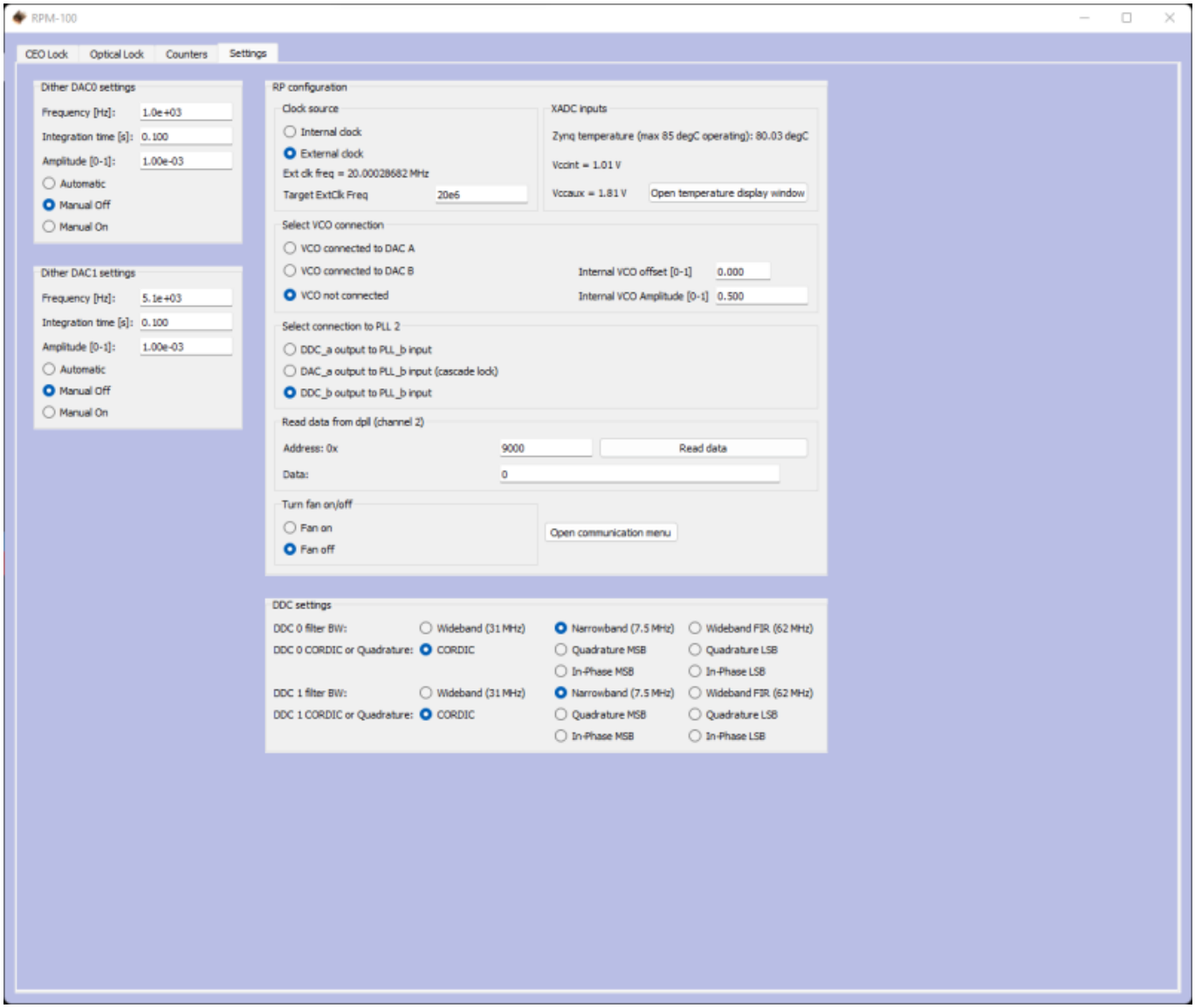


Fig. 9: The settings screen of the SLICE-FPGA-II

The SLICE-FPGA-II will attempt to use the specified frequency, however, due to the limitations of the FPGA's Peak Locked Loop hardware, certain frequencies work better than others. For example, frequencies such as 25MHz, 50MHz, 75MHz, 100MHz, 125MHz, or 200MHz will result in exact clocking and a clean 10MHz output signal. Unusual frequencies such as 42.3MHz cannot be used to produce a precise ADC clock or 10MHz reference.

Troubleshooting

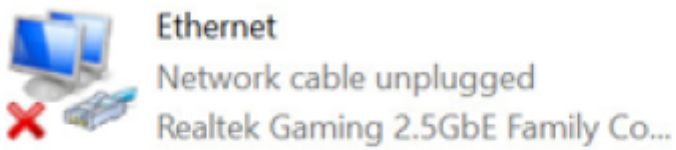
Overview

In many cases, all that is necessary to get up-and-running with the SLICE-FPGA-II is to install the correct WinPython distribution, and run the provided GUI software using the WinPython Spyder environment. If you are unable to connect the GUI to the SLICE-FPGA-II, follow the below instructions to eliminate possible causes of failure.

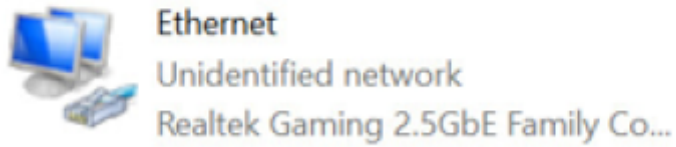
Ethernet Controller IP Configuration

Whatever ethernet port you use to control the SLICE-FPGA-II, it is necessary that your computer identifies itself on this Ethernet port with a fixed IP address in the **192.168.0.x subnet**. Sometimes a computer's default settings do not fit this requirement. From the Windows Control Panel, click through: Network and Internet –> Network and Sharing Center –> Change adapter settings

You will see a number of network adapters listed. You should see one of the network adapters change state when you connect the powered-on SLICE-FPGA-II to your PC via the ethernet cable, as shown below:



Before



After

Watch for this change to identify the correct network adapter.

- Right-click on the adapter, and click **Properties**.
- From the screen that appears, click on "Internet Protocol Version 4 (TCP/IPv4)" and then click Properties.

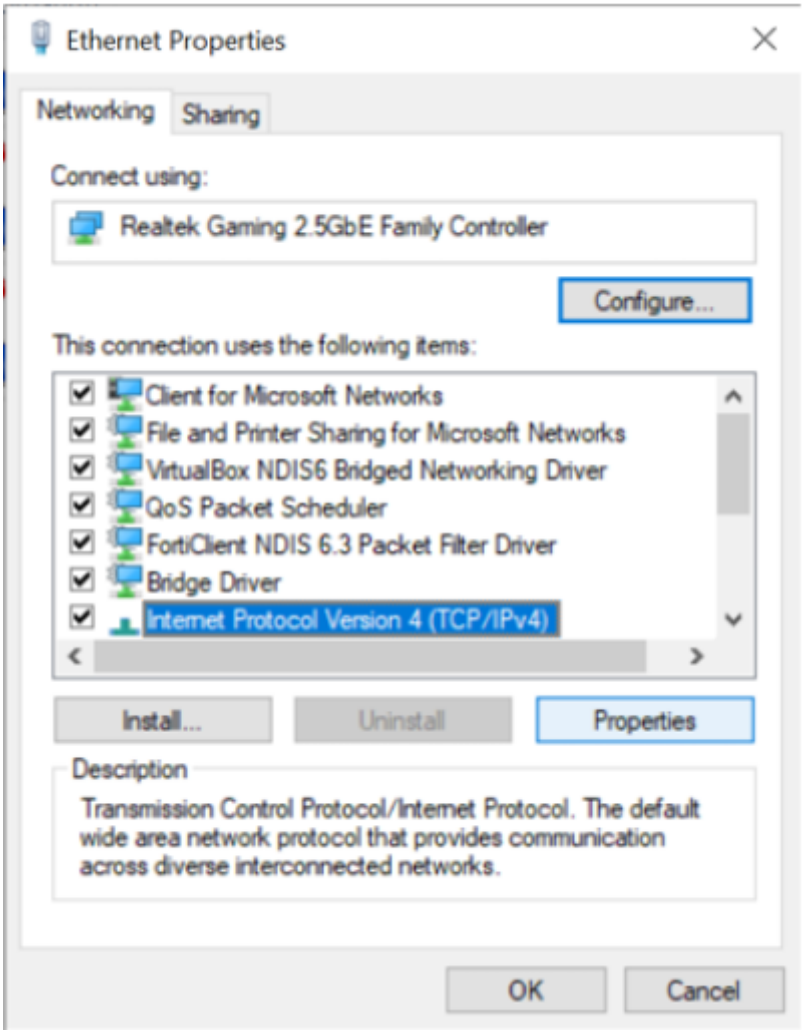


Fig. 10: The Adapter Properties screen, with the IPv4 Settings highlighted

- In the IPv4 Properties Page, select the bubble next to “Use the following IP address:”, and fill in the IP Address to be **192.168.0.xxx**, where **xxx** is an integer from 0 to 255, and not **150**, as that is the address used by the SLICE-FPGA-II. In this example, we used 196.

Fig. 11: The IPv4 Properties page, with the IP Address and Subnet Mask filled in.

The Subnet Mask will default to 255.255.255.0, which is fine.

NOTE: If you use this same Ethernet port to connect to another network, these configuration changes could result in connectivity problems with that network. If this poses a problem for you, consider buying a USB-to-Ethernet adapter, and configuring just that adapter for use with the SLICE-FPGA-II.

Windows Firewall Rules

If you continue to have trouble connecting to the SLICE-FPGA-II, it's possible that your firewall settings are blocking communications with the device. From the Windows Control Panel, click on System and Security –> Windows Defender Firewall –> Advanced Settings to open up the **Windows Defender Firewall with Advanced Security** manager application. In the left panel of the program, click "Inbound Rules." Then, in the right-hand panel of the program, click "New Rule..." Use the "New Inbound Rule Wizard" to create a new rule to the following specifications:

- Rule Type: **Program**
- Program: **[WINPYTHON INSTALL DIRECTORY]\WinPython-64bit-3.6.1.0Qt5\python-3.6.1.amd64\python.exe**
- Action: **Allow the connection**
- Profile: **Domain, Private, and Public**
- Name: **Red Pitaya WinPython** (or another name of your choice)

In the left-hand panel, click "Outbound Rules", and then click "New Rule...". Repeat the above Rule

creation steps to create a rule that allows outgoing packets from the WinPython directory's "python.exe" file. Finally, ensure that the aforementioned python.exe file is not being restricted by any other firewall rules.

1)

Do not exceed +10dBm for the protection of the device

2)

at 10MHz