SLICE-FPGA

Document Transfer

Copy the contents of the “NIST FPGA GUI” folder to local storage. There are five components needed to create the environment for the Comb GUI:

1. WinPython 2.7.10.3
2. Opal Kelly API
3. Python GUI and FPGA firmware
4. PyVISA.whl file
5. Opal Kelly Front Panel driver

Installation Process for SLICE-FPGA Software

1. Install WinPython 2.7.10.3 using the installer “WinPython-64bit-2.7.10.3”. Remember the installation directory.
2. Open a new file explorer window and navigate to the WinPython installation (wherever you just installed it) and open the folder \python-2.7.10.amd64\Lib\site-packages.
3. Copy the entire “ok” folder into the site-packages directory of the WinPython Installation.
4. Open a WinPython command prompt using the shortcut in the WinPython install directory. This provides a command prompt that has the proper path variables to run the GUI using the WinPython installation. Type the following:
    1. pip install {whl_file_dir}\PyVISA-1.8-py2.py3-none-any.whl.
    2. Press tab to cycle through the autocomplete options. Example:
    3. c:\users\osa\WinPython> pip install c:\users\osa\fpga\PyVISA-1.8-py2.py3-none-any.whl
    4. 3.5. Install the Opal Kelly Front Panel Windows Drivers by double-clicking “FrontPanelUSB-Win-x64-4.5.6”

FPGA Control

The SLICE-FPGA dual-channel Offset Phase Lock Servo can be used to phase lock f_{CEO} and f_{opt}. Locking f_{opt} requires a reference CW laser and heterodyne setup (such as a 50:50 beam splitter and DWDM filter). The stability of the lock will depend on the reference laser used. All performance data is collected with a Rio Planex laser.

If you have not already done so, install Python and the FPGA software for controlling the SLICE-FPGA dual Offset Phase Lock Servo.

Software Startup

1. Open a WinPython command window and navigate to the folder “GUI and Firmware”. Note that a WinPython command window is not the same as the Windows native CMD command line.
2. Start the SLICE-FPGA control GUI by typing “python XEM_GUI3_VPv4.py”, figure 1).

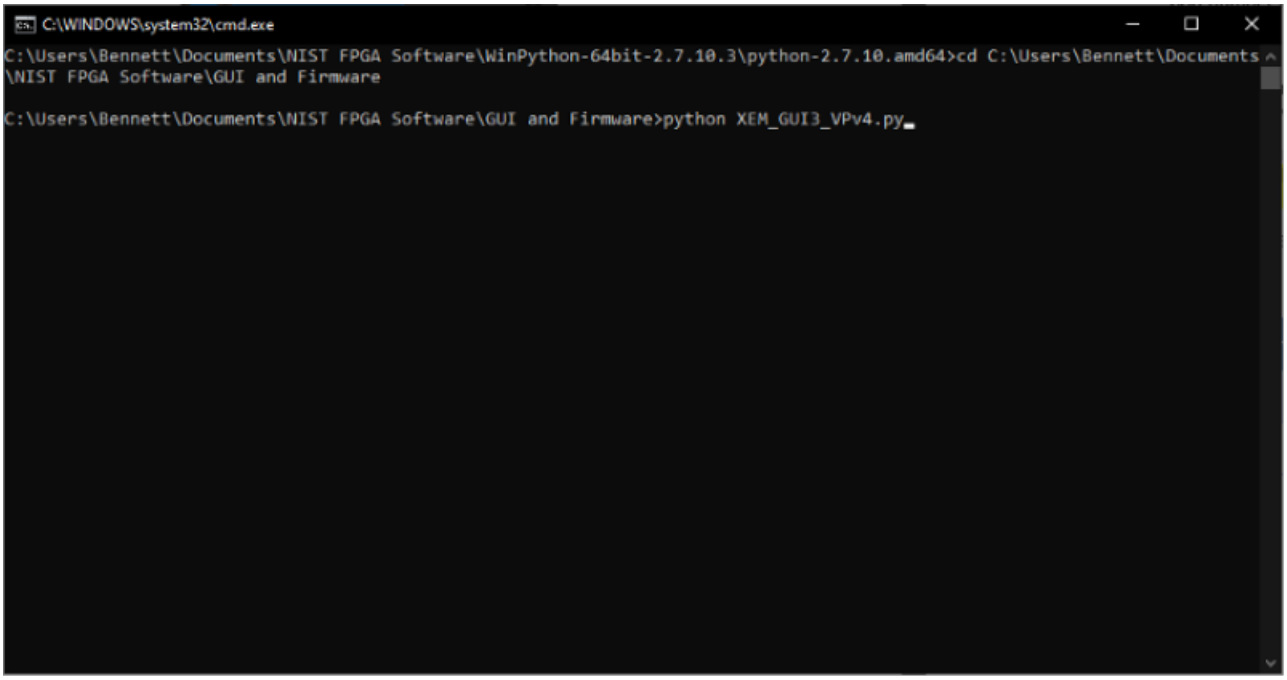

Fig. 1: Start FPGA GUI from Terminal

3. A start-up menu should appear (figure 2). Make sure “superlaserland_v12.bit” is selected and select an appropriate clock option: internal clock will use the FPGA's on board clock for timing, whereas external clock can be selected to allow synchronization between devices with a separate timing device. If you are unsure which to select, choose Internal Clock. Leave all other settings as default and press OK.

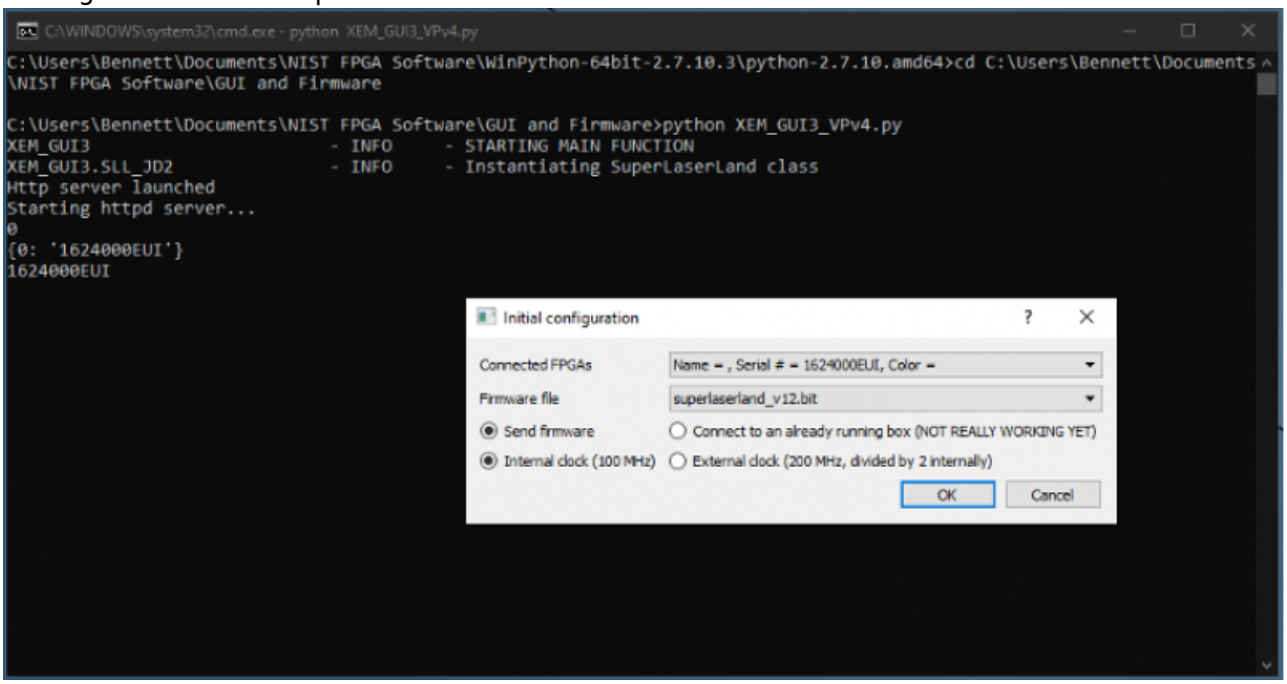

Fig. 2: FPGA GUI Start Screen

4. Navigate to the Filter Settings tab and select “Narrowband (6MHz)” for both DDC0 and DDC1 (figure 3).

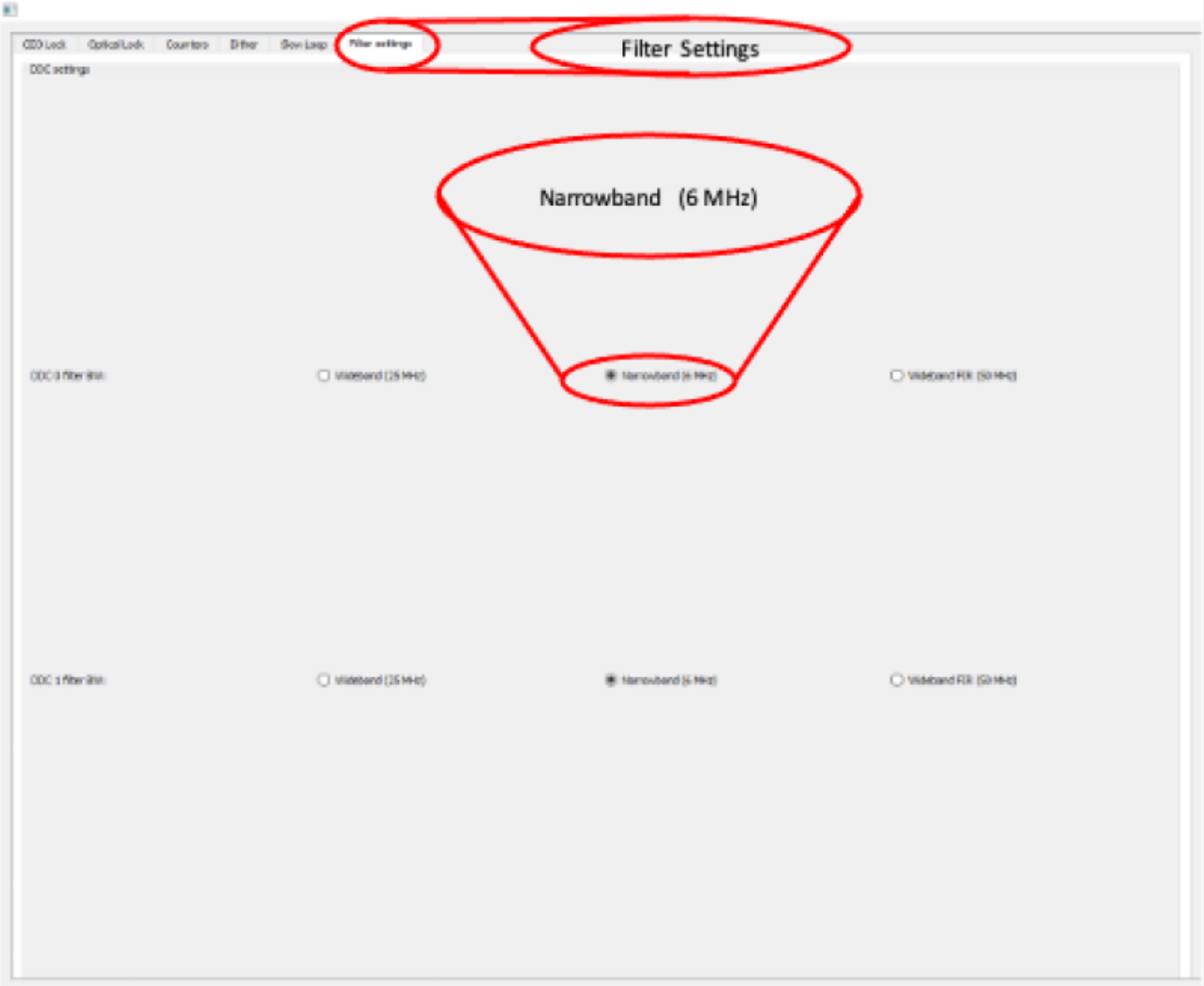

Fig. 3: Set Loop Filter Bandwidth

CEO Lock

This tab of the FPGA software allows the user to lock f_{CEO}, and to tweak the parameters of the lock for best performance. To lock f_{CEO}, first ensure that there is a visible beatnote displayed on the "Spectrum" plot. This will be an obvious peak above the noise floor which responds to adjustments of the "Offset DAC 0 [V]" slider. If a beatnote cannot be identified, check that the FFC-100 is mode locked. Once a beatnote has been identified, adjust the "Offset DAC 0 [V]" slider such that the Baseband IQ plot is roughly circular, or the identified beatnote is between two of the dips on the spectrum plot corresponding to a bandpass filter (figure 4). It is important to note that, while the "Offset DAC 0 [V]" slider range displays values between 0 and 8V, the DAC itself is incapable of going higher than 4V, so make sure that the slider is between 0V and 4V while making this adjustment. If the slider is placed higher than 4V it will not damage the system, but it might cause problems with obtaining a lock.

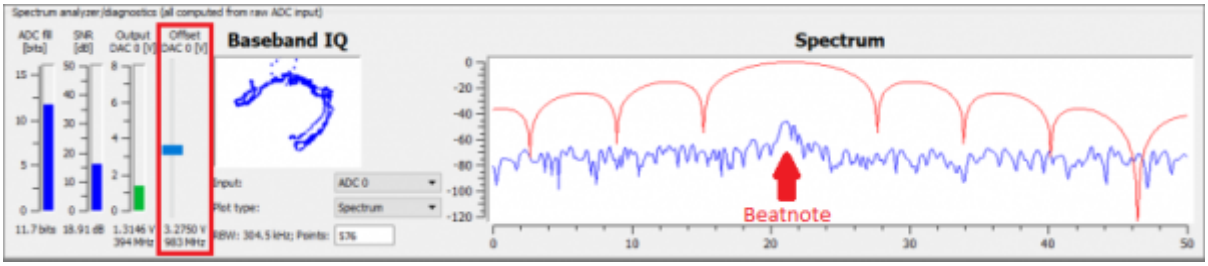

Fig. 4: Offset DAC location and Beatnote Example

To lock the system, simply click the checkbox at the top of the screen labeled “Lock” and the system should snap fairly quickly into a lock. If the system does not lock, and immediately rails, uncheck the “Lock” checkbox, change the sign of the VCO by selecting the opposite “VCO sign” checkbox to the right of the “lock” checkbox, and try again. If the system still does not lock, check that your PID parameters are set to, or near to, the values given in your CoC and shipped with the system. If there is still no lock, check the Troubleshooting section for potential solutions.

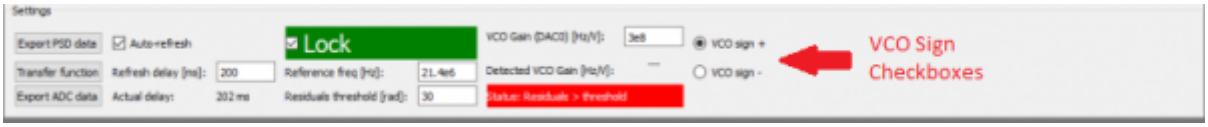

Fig. 4: Offset DAC location and Beatnote Example

Once a lock has been obtained, the green plot of phase noise on the “Phase Noise PSD, std dev =” plot will show a dramatic reduction in noise from f_{CEO}'s unlocked state. This number is a good characterization of the stability of your lock. A good lock of f_{CEO} is indicated by an integrated phase noise PSD less than 2 rad, but this value can be pushed down even further by adjusting the PID settings of your FFC-100.

Before adjusting the PID parameters, uncheck “Auto-refresh” at the top of the screen. Change the value of “RBW: 576 Hz; Points:” to “3e6”, then recheck “Auto-refresh” (figure 6). This will update the graph to plot more points and give a more accurate representation of the phase noise. It is important that Auto-Refresh be unchecked before making this adjustment, however, as doing so while the plot is refreshing may cause the FPGA software to crash. If this happens, simply relaunch the software and start again.

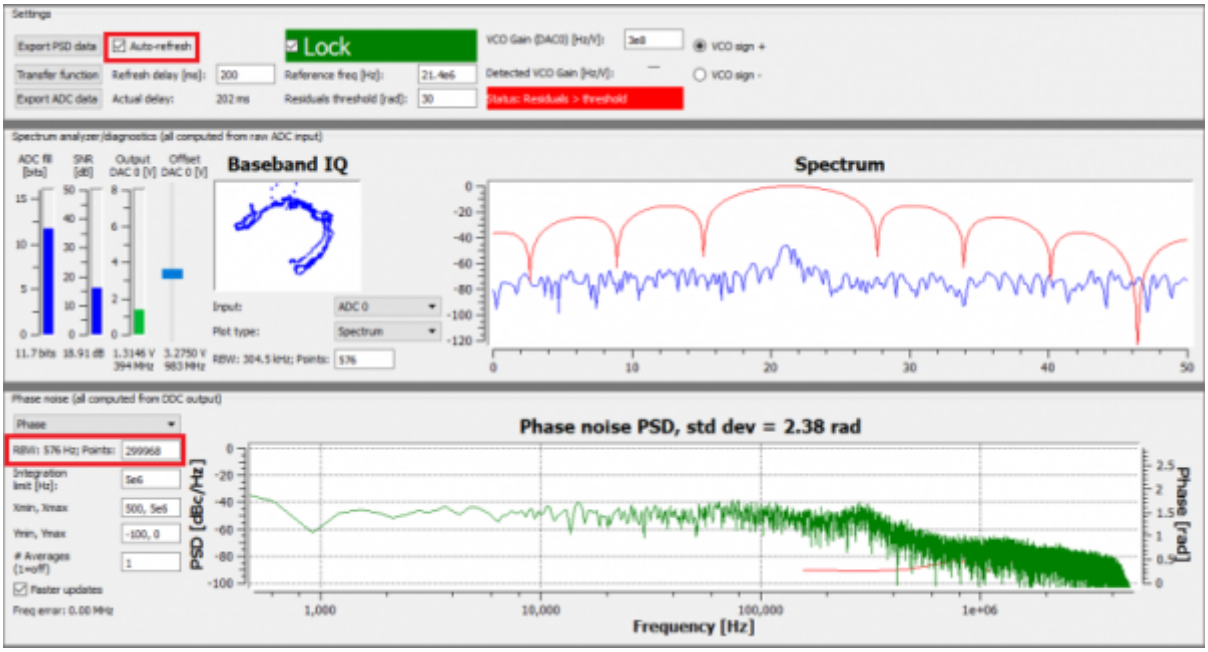

Fig. 6: Resetting the RBW and Plot Points to get more accurate phase noise plot

The PID settings provided with the FFC-100 on delivery are intended to give a relatively stable lock out of the box in normal laboratory conditions. If at any point the PID parameters are adjusted too far out of range and the FFC-100 is not locking, resetting them to ship parameters will allow you to quickly get back to a baseline lock. The PID parameters shipped with the FFC-100 can be found in section 6 of CoC delivered with your FFC-100.

Adjustment of the PID settings to obtain a tighter lock can be done from the bottom section on the CEO lock tab (figure 7). Begin by resetting the parameters to ship settings, and then adjust Kp by clicking on its slider, then pressing the arrow keys on your keyboard. It is possible to move the slider with the mouse, or by typing in a value, but the keyboard arrow keys will provide the most fine tuned control of the value. Change the value up or down and watch the number displayed in the Phase Noise PSD plot to ensure that the changes are reducing integrated phase noise. After optimizing Kp, if the integrated phase noise is still too high, go through the other PID parameter sliders underneath until you have reached your desired noise optimization. In general, small adjustments of Kp will provide the largest change in integrated phase noise, assuming that all values begin close to ideal.

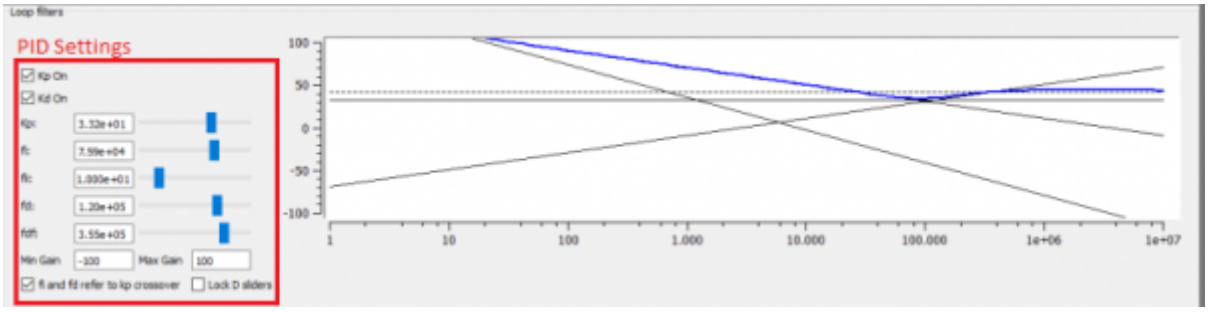

Fig. 7: PID Control sliders

Optical Lock

This tab allows the user to lock and tweak f_{opt}: the beatnote between a tooth of the FFC-100 and the reference laser. The process for locking f_{opt} is nearly identical to locking f_{CEO}, except that there is an extra slider (Offset DAC 2) on the screen. It has no effect on the system, and can be left alone. Begin by adjusting the “Offset DAC 1 [V]” slider until the Baseband IQ is roughly circular, or the beatnote is

positioned between two dips on the Spectrum plot corresponding to a band pass filter. Once the beatnote is centered, or the Baseband IQ is roughly circular, check the “Lock” checkbox at the top of the tab and wait a moment. The Phase Noise PSD plot will indicate whether your system is locked by showing a dramatic reduction in noise, and integrated phase noise. If your system is railing, change your VCO sign by selecting the opposite “VCO sign” checkbox to the right of the “Lock” checkbox. To optimize your lock, follow the instructions for adjusting PID settings given in the CEO Lock section.

On both the CEO Lock, and Optical Lock tabs, it is possible to change what is being plotted on the Spectrum graph in the Spectrum analyzer/Diagnostics bar. To do so, simply click on the “Plot type:” drop down menu and choose what you would like to plot. The options for this menu are: Spectrum, Time: raw input, Time: phase, Time: IQ, and Time, IQ synced. Choosing any option besides “Spectrum” will change the units on the bottom of the plot from Hz to seconds, and give a live plot of the value selected in the time domain. The same can be done with the Phase noise PSD plot in the Phase noise bar by clicking on the drop down menu in the top left hand corner of the bar (figure 8). The options for the Phase noise PSD plot are: Frequency (Freq), Phase, and time domain versions of each respectively. Other options for this plot include setting the outer limit for PSD integration scalable X and Y axes, and averaging. When taking a measurement of Phase noise or integrated PSD, it is recommended that the Averaging field be set to no less than 10.

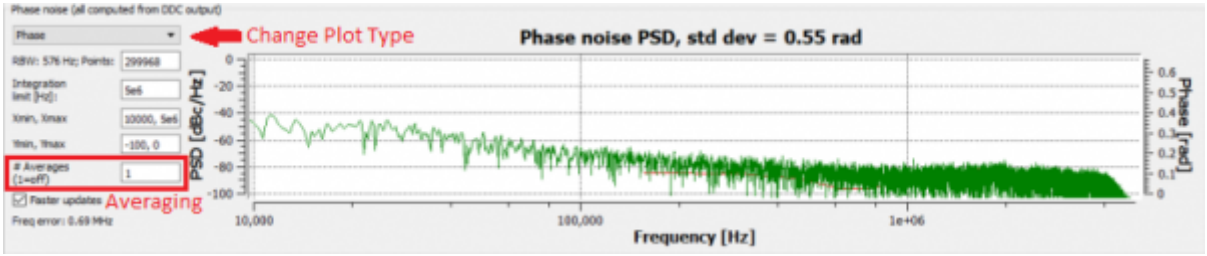

Fig. 8: Several options are available for how the Phase noise PSD plot is displayed.

To export data from the FPGA to a file, simply press one of the two export buttons in the Settings bar at the top of the tab(figure 9). If ADC data is being exported, a pop-up will appear and ask the user which ADC to export. The files will be saved in csv format to the Software and GUI folder from which the FPGA software is launched under data_exports. If this folder does not exist in that location, it will be created the first time data is exported.

Fig. 9: Export ADC data, or the Phase noise PSD chart to CSV

Specific settings pertaining to the the way the loop filters are engaged to obtain the optical lock are available in the Loop Filters bar at the bottom of the Optical lock tab. It is not advised that the settings for this section be changed from their default values. Doing so could affect your ability to obtain a stable lock.

Dither

The Dither tab allows the user to add a modulation to the DAC current. Each DAC can individually be configured to be modulated at a specific frequency, integration time, and amplitude. A checkbox

below these fields allows the user to select whether the modulation is always on (Manual On), always off (Manual Off), or to allow the computer to determine when the modulation is applied (Automatic).

Slow Loop

Firmware Version FL-V1.2

The Slow Loop tab allows the user to enable a slow servo temperature control of the intracavity PZT to prevent offset drift over long periods of time. It is recommended to always enable this feature after setting up a lock, as without it the PZT's offset voltage can drift to its rails over the course of several hours or even less. To enable the Slow Loop feature, simply fill in the “FFC COM Port:” field with the number corresponding to your FFC-100's COM port, choose the desired setpoint of the PZT, and press the “Activate Temperature Slow Loop” button at the top of the tab. For example, if your FPGA is on COM4, and your FFC-100 is on COM8, type “8” into the “FFC Com Port:” field and then press the button. This will bring up a command prompt window which will display information about the Slow Loop, such as the cavity temperature, and the current PZT setpoint. In general, it is best to select a setpoint near the center of the PZT's available range.

To determine the COM port of your FFC, open the Windows Device Manager on your PC, expand the “Ports (COM & LPT)” drop down, take note of which COM ports are listed, then unplug the FFC-100's USB connection. After the list updates, the COM port of the FFC-100 will no longer be listed.

Filter Settings

The Filter Settings tab allows the user to change the type of band-pass filter which is applied to the locking DACs (DAC 0 for f_{CEO} and DAC 1 for f_{opt}). Each DAC has three options: Wideband (25 MHz), Narrowband (6 MHz), and Wideband FIR (50 MHz). Before attempting to lock either f_{CEO} or f_{opt}, it is suggested that the Narrowband filter be selected for both DACs.