Fiber Frequency Comb Module Quick Start Guide

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Please read Limited Warranty and General Warnings and Cautions prior to operating the FFC-CM.

Fig. 1: The FFC-CM with a coffee mug for scale

Links

Vescent manuals page.
FFC-CM Laser Driver API.
FFC-CM Fiber Laser/Oscillator API.
I2C API interface
FFC-CM web page.

Please check back for added functionality. Contact sales [at] vescent [dot] com for questions and corrections, or to request added functionality.

Purchase Includes

- FFC Comb Module
- Power cord for your country (if known)
- Instructions on how to download & install control software
- Final Test Documentation
- Other items depending on specific configuration

A List of Included Items Would be Swell

List of Warning Symbols

	Warning. Pay special attention to procedures and notes. If procedure is not followed carefully, damage to the FFC-CM or devices connected to it may occur.

	Potential for electrical shock hazard.

Absolute Maximum Ratings and Power Input

Note: All modules designed to be operated in a laboratory environment.

Parameter	Rating
Environmental Temperature	>15°C and <30°C
Environmental Humidity	<60%
Environmental Dew Points	<15°C
Maximum CW In Optical Power	2 mW
Maximum OSC In Optical Power	XX
Maximum AMP 1 In Optical Power	XX
Maximum AMP 1 In Optical Power	XX

Tab. 1: Absolute Maximum Ratings

Proper Usage

	If this instrument is used in a manner not specified by the manufacturer in this manual or other relevant literature, protection provided by the instrument may be impaired.
	Successful implementation of the FFC-CM depends critically on the design of the whole system: FFC-CM, phase locking electronics, and any references to which the FFC-CM is locked or *vice versa*.

Notice

	Do not block the airflow vents on the side of the chassis or the fan inputs & outputs on either the FFC-CM or the SLICE-FPGA.
	Keep the oscillator current within the range specified in your product's final test documentation or CoC.

Acronyms, Abbreviations, & Definitions

Jargon	Meaning
CoC	Certificate of Conformity- collection of performance data for a specific unit as measured by the factory during the manufacture of the unit. Final Test report.
EDFA	Erbium Doped Fiber Amplifier - the type of fiber amplifier used in the FFC-CM.
SC	Supercontinuum - The octave-spanning light used for self-referencing.
PM LC/APC	Polarization Maintaining Local Connector/Angled Physical Contact connector.

Tab. 2: Terms Defined

Features

Front Panel

A labeled diagram of the front panel is shown in figure 3. The functions and connections are as follows:

Fig. 2: DC Power Connector Pinout

Pin	Signal	Mating Harness Wire Color (TE Connectivity T4161320005-002)
1	+5V_RTN*	BROWN
2	+5V	WHITE
3	+15V	BLUE
4	-15V	BLACK
5**	15V_RTN*	GRAY

* Returns are galvanically connected.

** Pin 5 is center pin.

1. PZT Modulation Input (From FPGA)
2. Digital Control (DB-9 I^2C/UART)
3. DC Power Input (figure 2)
4. f_{CEO} Output Monitor (SMA)
5. f_{opt} Output Monitor (SMA)

6. f_{rep} Output Monitor (SMA)
7. Oscillator Pump Input (PM LC/APC)
8. Amplifier 1 Pump Input (PM LC/APC)
9. Amplifier 2 Pump Input (PM LC/APC)
10. CW Laser Reference Input (PM LC/APC)
11. Internal Oscillator Output (PM LC/APC)
12. Supercontinuum Output (PM LC/APC)

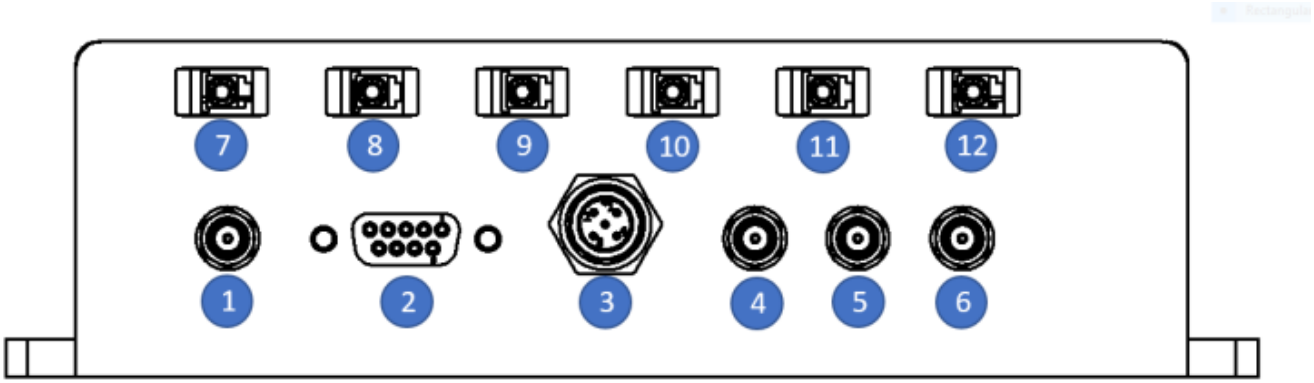

Fig. 3: Front of FCC-100

Rear Panel

A labeled diagram of the rear panel is shown in figure 4. The functions and connections are as follows:

1. Mini USB Serial Communication Port

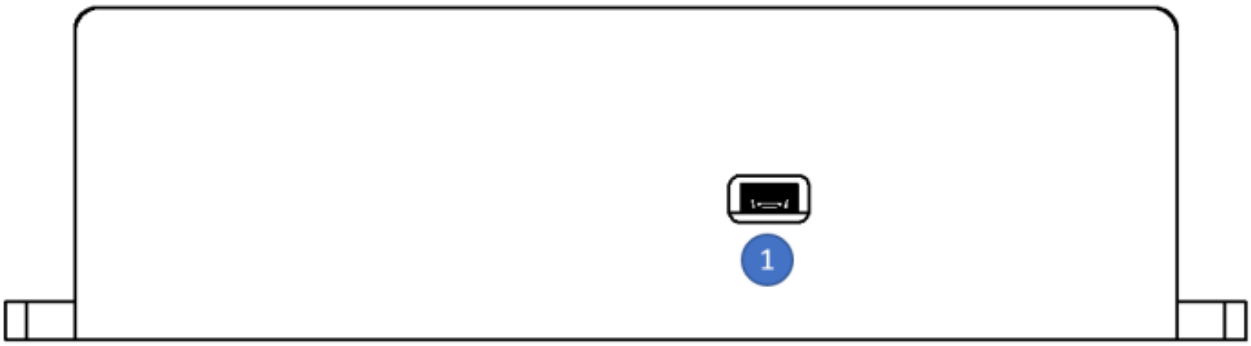

Fig. 4: Front of FCC-100

Operating the FFC-CM

This document provides basic instructions on how to operate the Vescent Photonics Fiber Frequency Comb Module in conjunction with the Vescent SLICE-FPGA. It is important to note that the FFC-CM itself does not come with a built in GUI, and as such communication must be done through the Serial Command API or the FPGA Software. This document will walk through usage of the Serial Command interface including several basic commands, as well as using the FPGA Software to obtain and optimize your lock.

System Set-up

Initial Connections

To begin, connect the FFC-CM to power, turn it on, then connect it to a Windows 10 computer using the included Mini USB to USB Type-A connector. The next few steps will walk through installing and verifying the SSH software required to communicate with the FFC-CM.

Serial Command Interface

To use the FFC-CM, you will first need to install SSH software for communicating via serial commands. Vescent recommends using either Tera Term or PuTTy, but there are a variety of other options. This guide will focus on connecting to the FFC-CM using Tera Term.

Installing SSH Software

To download Tera Term for Windows 10, follow this link, and click on the .exe file for the latest release (see figure 5). You will be redirected to another page, where your download will begin automatically. Once the download is complete, launch the application from the downloads folder, and follow the instructions to configure Tera Term on your device. You do not need to select or deselect any of the optional packages.

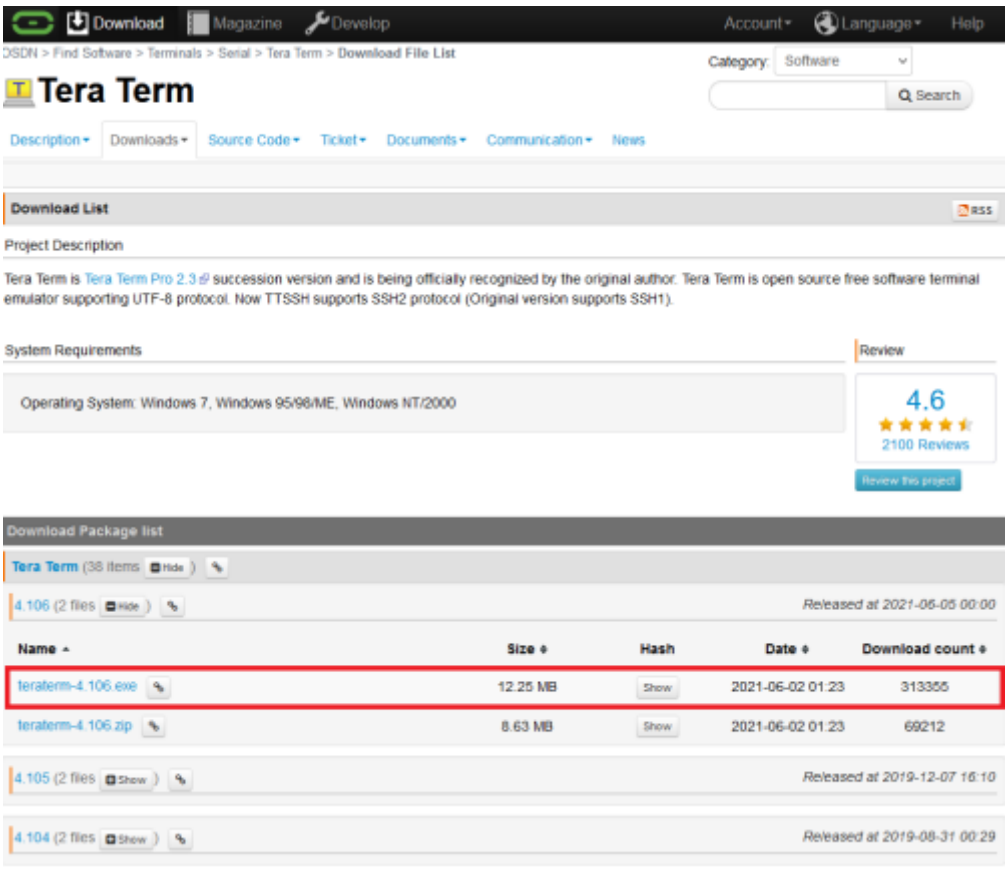

Fig. 5: Tera Term Downloads Page

Connecting to the FFC-CM

Once Tera Term is finished installing, launch the application. You will be shown a window like the one in figure 6. Check the “Serial” option and select the COM Port associated with your FFC-CM. To find the correct COM Port, open the Device Manager, and expand the “Ports (COM & LPT)” drop-down. Unplug the Mini USB to Type-A connector while watching the list of devices. The COM Port of the FFC-CM will be the one that disappears. Plug the USB cable back in and select the correct COM port, then click “OK” in the window.

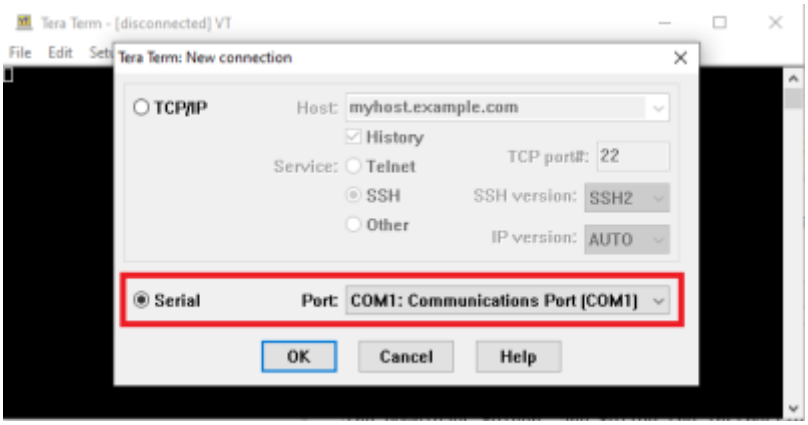

Fig. 6: Initial Tera Term Window

Next, navigate to “Setup –> Serial Port...” in the menu bar at the top of the window and change the “Speed” from 9600 to 115200. Click “New Setting” to save. Then navigate to “Setup –> Terminal...” and change both “Receive” and “Transmit” from “CR” to “CR+LF”. Check “Local Echo” and then click “OK” to save the settings. After configuring the terminal, you may choose to save the settings for import later. To do so, navigate to “Setup –> Save Setup...” and choose a location to save the file. When you launch Tera Term the next time, simply choose “Setup –> Restore Setup” and load the file you saved earlier.

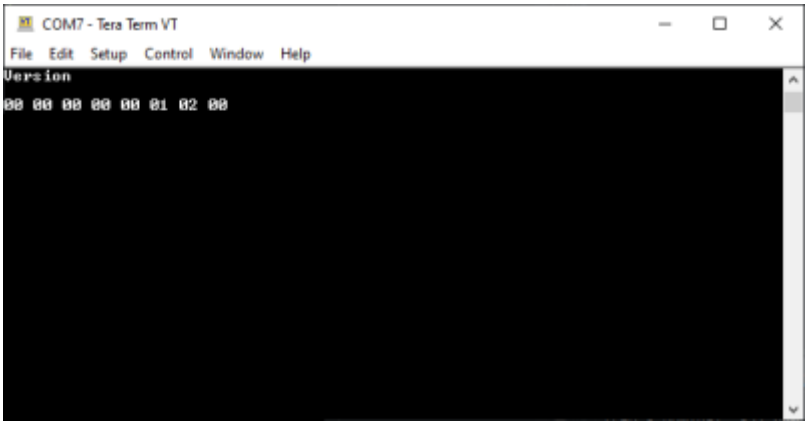

Fig. 7: Verify that the FFC-CM is communicating with the Version command

Finally, type `Version` into the terminal and hit enter to verify communication with the FFC-CM as shown in figure 7. If the connection was successful, the return will be 8 bits showing the firmware version on the FFC-CM.

Sending Commands

With the Serial Command interface set up, you will now be able to send individual commands to the FFC-CM over USB by typing them directly into the terminal. During the initial verification and test setup of the FFC-CM, it is recommended to use the terminal interface as shown in this guide, though later it may be beneficial to write your own serial command scripts.

FPGA Control

The SLICE-FPGA dual-channel Offset Phase Lock Servo can be used to phase lock f_{CEO} and f_{opt}. Locking f_{opt} requires a reference CW laser. The stability of the lock will depend on the reference laser used. All performance data generated at Vescent is collected using a 1556.2 nm Rio Planex Laser as the CW reference laser.

Installing FPGA Software

To use the FPGA software you must download both WinPyton and the FPGA software onto a control laptop or desktop computer. No additional firmware needs to be installed on the FFC-CM itself. To install the FPGA software, follow this link, click on “FPGA Software.zip”, and then press the download button. Make sure to save the zip file to your computer, and not just open it. Extract the file to a directory which will be convenient to navigate to using a command line.

Next, install WinPython version 2.7.10.3 by following this link and choosing the appropriate file for your system. Do **not** download the latest version of WinPython, as it will not work with the FPGA software.

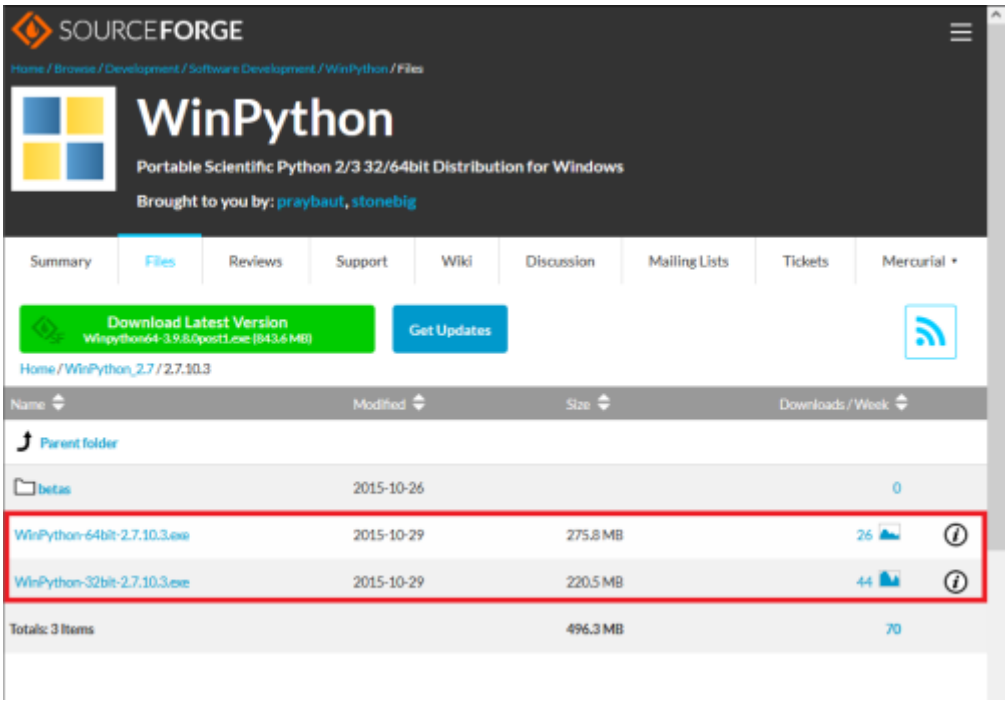

Fig. 8: Download Screen for WinPython. Choose one of the two options from within the red box.

To check which of the two files is correct for your system, go to the windows search bar or hit the

“Windows” key on your keyboard, and type “About your PC”. The window shown in figure 9 will appear, and you can find whether your computer is 32-bit or 64-bit. Choose the corresponding file from the download list in figure 8.

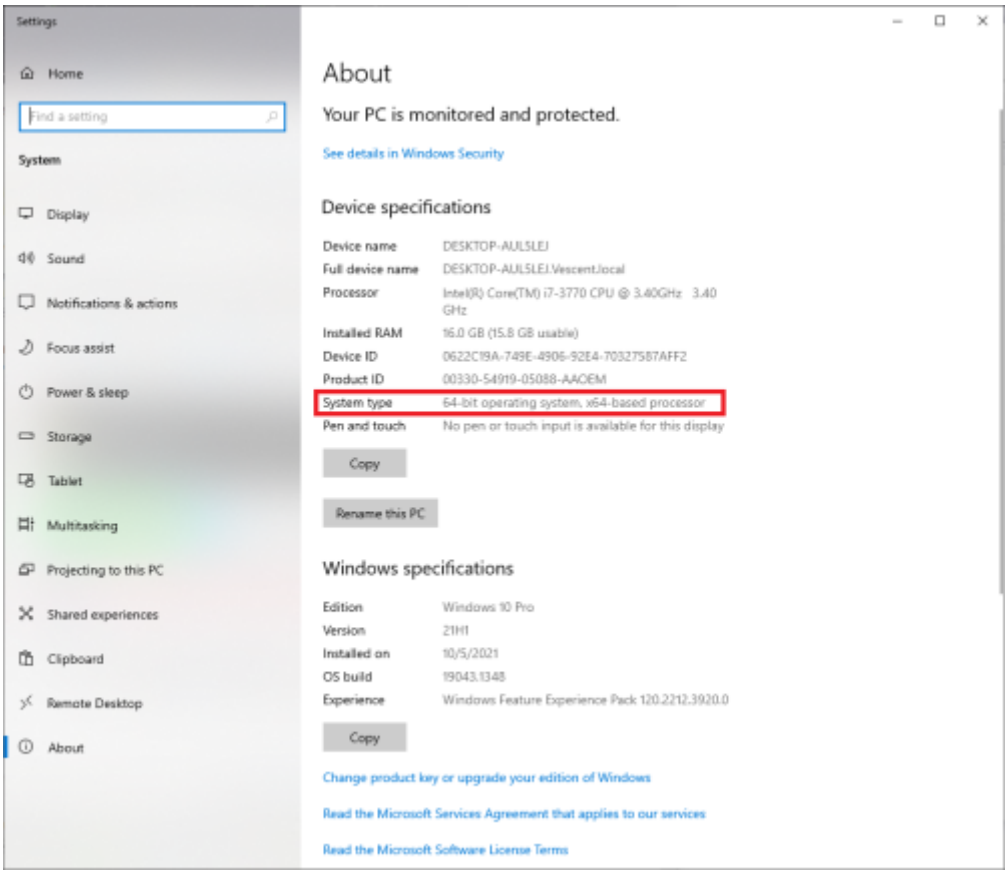

Fig. 9: Check whether your operating system is 32-bit or 64-bit

Once the download is complete, extract the file to a convenient location, and then navigate to the …`\python-2.7.10.amdXX\Lib\site-packages` folder, where XX is either 32 or 64 depending on which version you installed. In a separate file explorer window, navigate to your FPGA Software folder, and copy the entire “ok” directory from it into `\python-2.7.10.amdXX\Lib\site-packages`

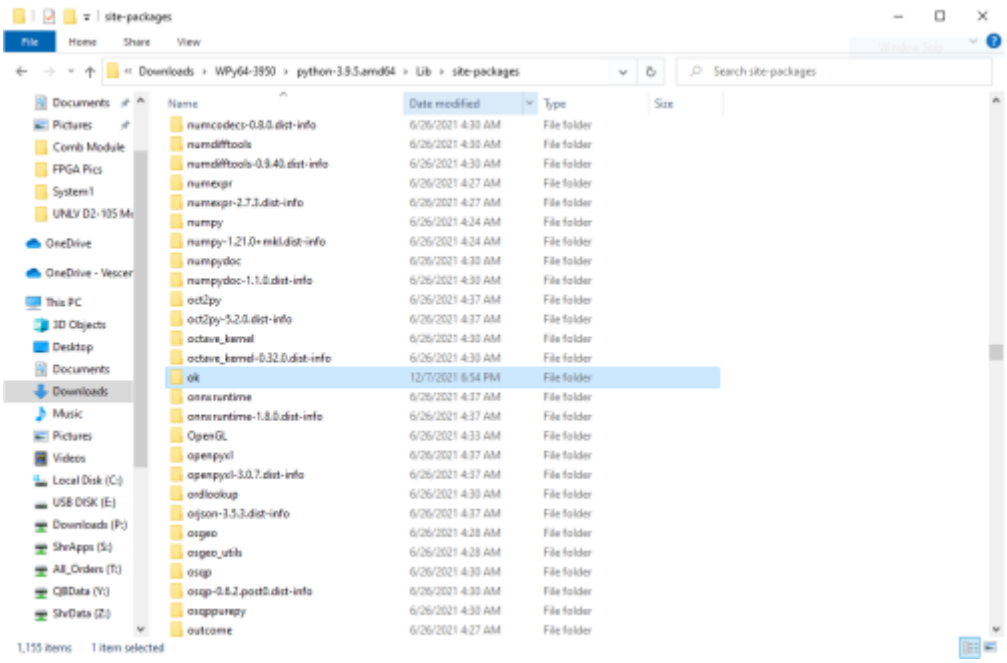

Fig. 10: The "ok" directory should be placed in this folder like shown here.

Back out to the WinPython root folder which you extracted and launch the “WinPython Command Prompt”, then type `pip install {whl_file_dir}\PyVISA-1.8-py2.py3-none-any.whl` but do not hit enter. Instead, use the TAB key to cycle through autocomplete options until you find “FrontPanelUSB-Win-x64-4.5.6”.

This part of the WinPython doesn't make sense to me. I'll ask Bennett about what you're supposed to do. Ignore that the rest of this section is missing.

Locking the FFC-CM

Before locking, it may be beneficial to familiarize yourself with the full list of API commands for the FFC-CM Laser Driver Board and Oscillator Board, as well as the front and rear panel connections, which can be found here. It is also important to note that, aside from those set in the FPGA software, all PID parameters come preset and should not need to be adjusted.

Connections

After initial verification of the FFC-CM with Tera Term, the system as a whole can be connected as shown in figure 12 with the exception of the pump diodes and CW laser. The USB “Optional Programming Interface” labeled “13” should already be connected to a Windows 10 machine, and should be left connected for the duration of this setup. Ensure that the FPGA remains off until Step 7. In general, do not power on any components of the system until explicitly instructed to do so. Failing to follow the correct start-up order may damage your system.

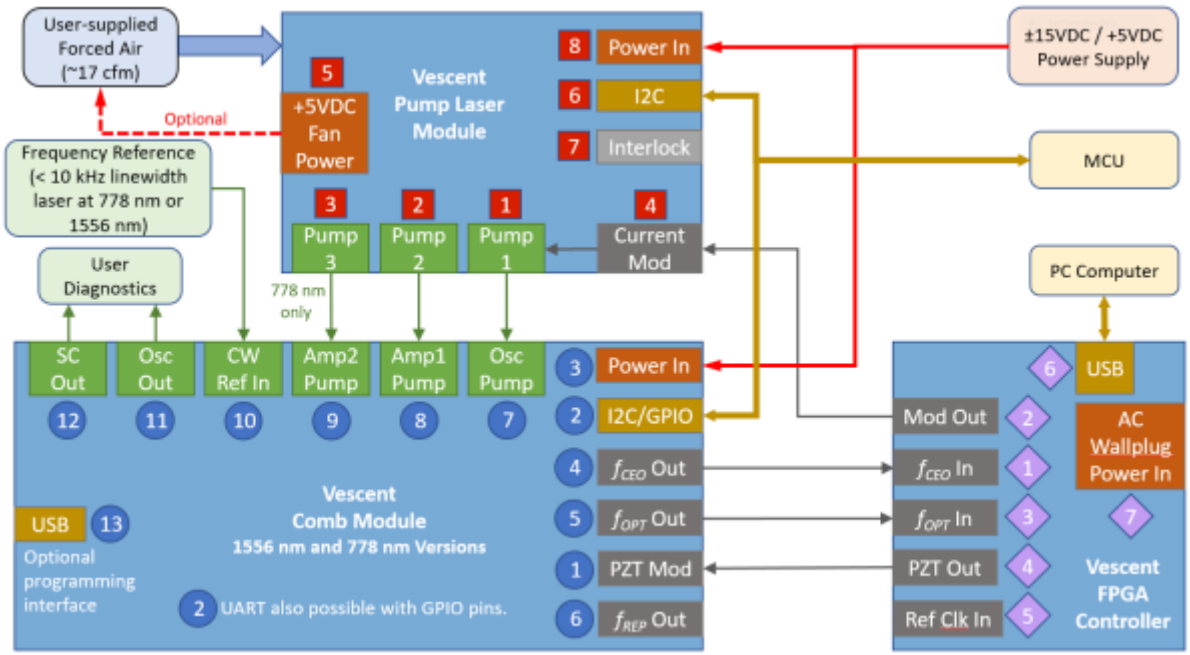

Fig. 12: High Level Block Diagram of FFC-CM system

Step 1: Turn on TEC and HV PZT

In the Tera Term terminal window, type `Tempset? 0` to check the setpoint temperature. If the return is not within the normal operating range of 20°C to 30°C, change the setpoint temperature to 25°C by typing `Tempset 0 25.0`. Next, enable the oscillator cavity TEC by sending the `Control 0 3` command and turn on the HV PZT by sending `Control 1 3`. It is not necessary to program a Bias Voltage on the FFC-CM, as the FPGA will add a bias voltage on its own. Finally, wait 5-10 minutes for the TEC to stabilize. The current temperature of the TEC can be monitored with the `Temp? 0` command, and the error between the temperature and the setpoint temperature (in mK) with `Terror? 0`. The TEC is stabilized when `Terror? 0` returns a value less than 0.1 mK.

Step 2: Power Pump Diode Boards

The actual I^2C implementation of the Pump Diode board has been left to the user, but in general it is at this time that the pump diode boards should be powered on and temperature stabilized. Do **not** supply current to the diodes themselves until their temperature has stabilized. The basic procedure for enabling the pump diodes is the same as that for the OSC board. First check the temperature of each laser driver board using the I^2C equivalent of [#28] `Tempset? 0`, then enable the TEC with the [#16] `control 0 3` command. Check the current setting for each laser driver board with [#106] `CCurset? 1` before enabling it. A list of available commands, as well as a description of the I^2C API can be found here.

After the pump diode temperatures have stabilized, it is recommended to check their output power at the current suggested in the CoC. Do not plug in pump diodes to FFC-CM system until you are satisfied that the output power of the diodes will not harm the system at their setpoint current.

If satisfied that the output power of the pump diodes is safe, ensure that the pump fiber ends are clean using a fiber cleaner, then connect the OSC Out (Pump 1) and any EDFA Amplifiers (Pumps 2 and 3) on the Pump Diode Board to the FFC-CM as shown in figure 12. If you're using the 1556nm system, there will only be one amplifier pump diode. If you're using the 778nm system, there will be two amplifier pump diodes.

Step 3: Power and Connect CW Laser

It is essential that the FFC-CM be locked to an external reference, which should now be powered on and connected to the FFC-CM as shown in figure 12. Follow the start-up procedure for your given CW reference laser.

The maximum power input for CW in is 2mW. Exceeding this input power may damage your system. Always check the output power of your CW reference before connecting it to the FFC-CM.

Step 4: Mode Lock the FFC-CM

Connect the OSC Mon output to an OSA. Check that the OSC pump diode's current setting is within the specified range of your CoC, and then enable current. It is recommended to start near the middle of the specified current range, and then to increase the current until CW breakthrough can be observed on the spectrum in the form of a narrow peak forming above the broader curve. Once CW breakthrough is achieved, lower the current roughly 20 mA to give the system room to modulate for a lock.

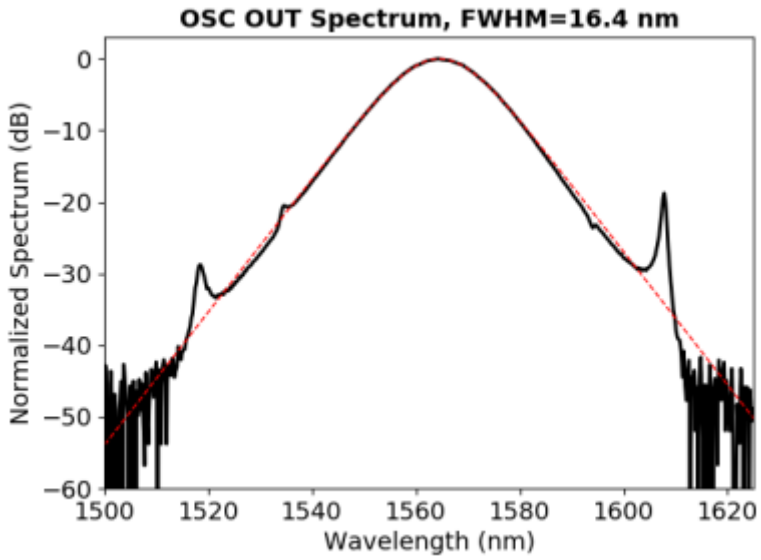

Fig. 13: Example spectrum showing a mode locked system

Should the current be increased too far, it is possible to enter a different mode locking regime. This will appear on an OSA as the spectrum suddenly becoming visibly narrower than before. Should this occur, incrementally lower the current until the laser jumps back into the previous, wider, mode locking regime. There is a slight hysteresis in this process, so it is likely that you will need to lower the OSC pump current past the current where the regime changed and nearer the middle of the specified current range.

Step 5: Verify Supercontinuum

Now that the system is mode locked, switch the monitored output to SC Out and change your OSA's window to span the 1-2 micron wavelength region. Verify that the supercontinuum of your system matches the one shown in your CoC. An example supercontinuum can be seen in figure 14

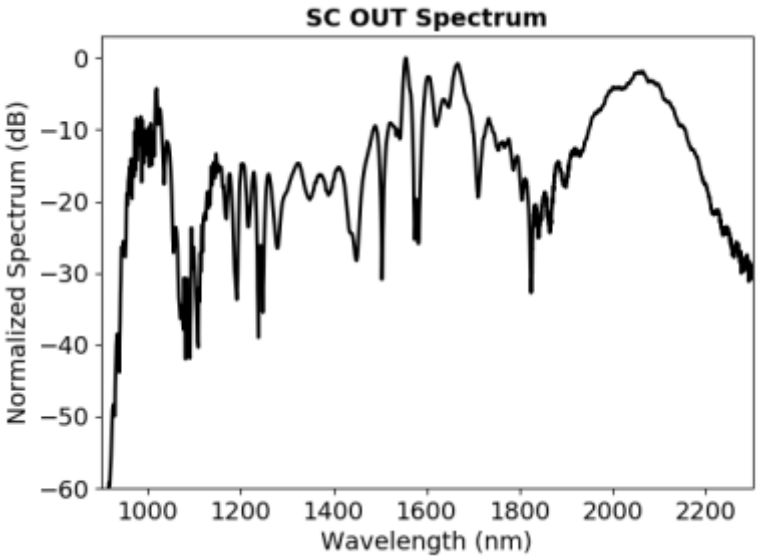

Fig. 14: Example supercontinuum of the FCC-CM system

Step 6: Verify RF Output

Connect the RF Mon output to a spectrum analyzer to verify that the RF output matches what is shown in your CoC. Set the spectrum analyzer's span to 1kHz-2GHz and look for a series of equally spaced peaks as shown in figure 15. The first peak is the repetition rate of your FFC-CM, and the rest are harmonics.

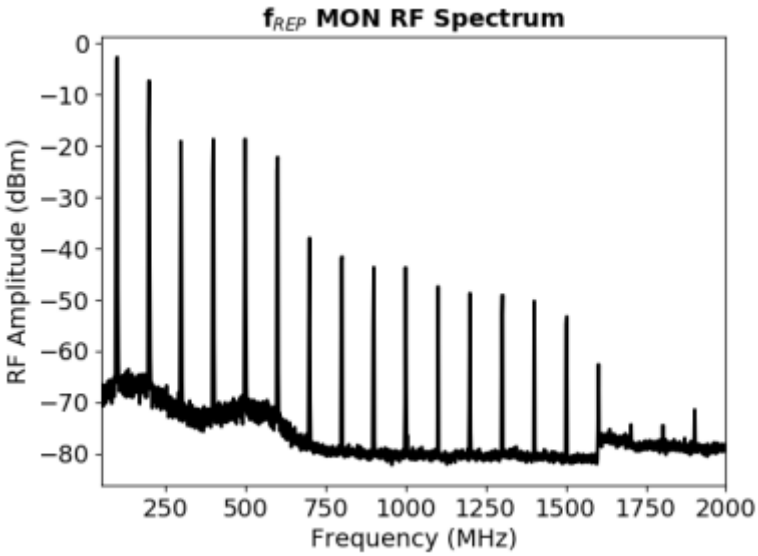

Fig. 15: Example RF spectrum from the FFC-CM system with 100 MHz repetition rate

Step 7: Power On and Set Up the FPGA

After verifying the outputs of the FFC-CM, make connections to the FPGA as shown in figure 12 if they have not been made already, and turn the FPGA on. The FPGA will apply a modulation current to the oscillator, which if not accounted for properly in Step 4 may cause your system to leave its mode lock regime.

The FPGA will apply an offset voltage to both the PZT Mod In and Current Modulation inputs upon start up. Therefore, the oscillator current set-point will have to be lowered accordingly and may need to be reset to the fundamental mode-locking regime.

Open a WinPython terminal and navigate to the …\“FPGA Software”\“GUI and Firmware” folder then run `python XEM_GUI3_VPv4.py` to launch the FPGA software. A window will appear asking for initial configuration settings as shown in figure 16. Ensure that “superlaserland_v12.bit” is selected for Fimware File, and check the “Send Firmware” and “Internal Clock (100 MHz)” boxes.

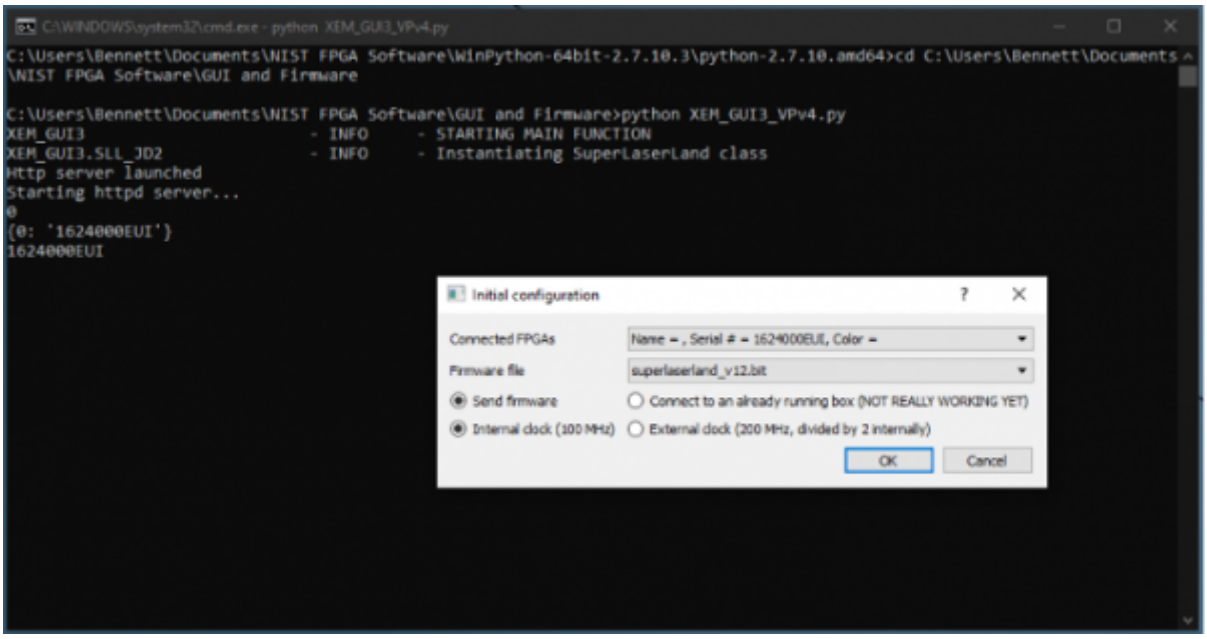

Fig. 16: Configuration window shown before FPGA software launches

Once the FPGA software launches, navigate to the “Filter Settings” tab and select “Narrowband (6MHz) for both channels. Finally, navigate to the “CEO Lock” tab, and input the PID parameters given in your CoC, then repeat for the “Optical Lock” tab.

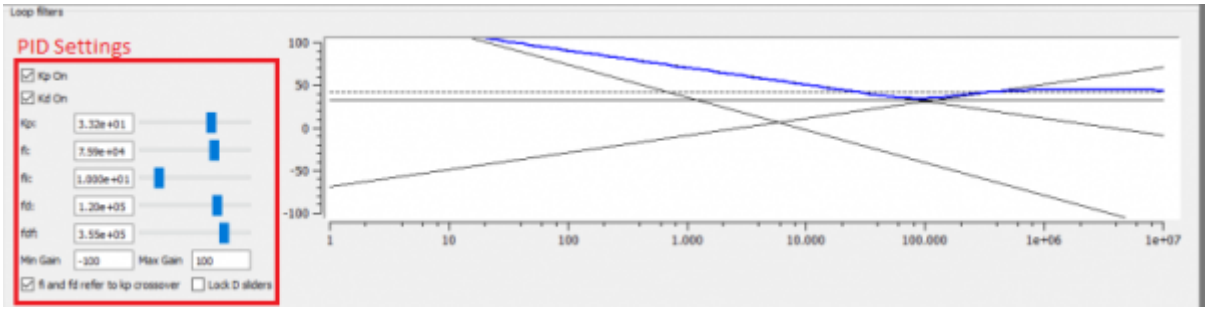

Fig. 17: Location of CEO Lock PID parameter input fields

Step 8: CEO Lock

Begin by navigating to the CEO Lock tab, then ensure that there is a visible beatnote displayed on the “Spectrum” plot. This will be an obvious peak above the noise floor which responds to adjustments of the “Offset DAC 0 [V]” slider as shown in figure 18. If a beatnote cannot be identified, check that the

FFC-CM is still mode locked. Once a beatnote has been identified, adjust the “Offset DAC 0 [V]” slider such that the beatnote is centered within the red bandpass filter spectrum.

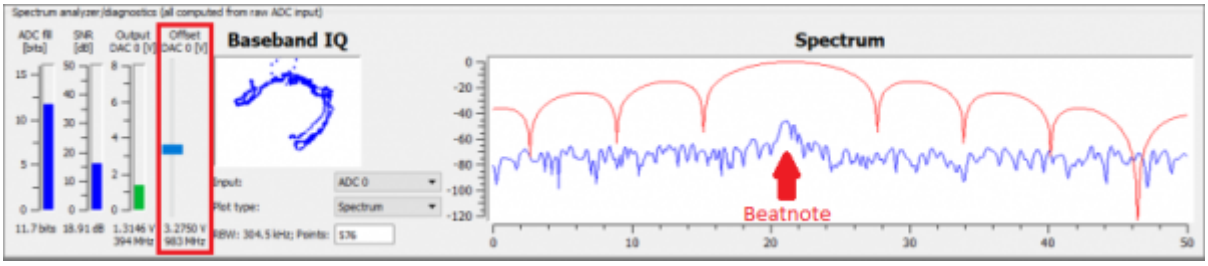

Fig. 18: Offset DAC location and Beatnote Example

Determine the VCO sign of the system by very slightly increasing the “Offset DAC 0 [V]” slider. If the beatnote moves to the right the sign is positive. If it moves to the left the sign is negative. Check the appropriate VCO Sign checkbox shown in figure 19, then press the “Lock” button. The system should quickly lock up, but if it doesn't, check the opposite VCO sign check box and try again. If the system still does not lock, double check that the PID parameters were set to the values shown in your CoC, and finally, try lowering the value of Kp by 10-20%.

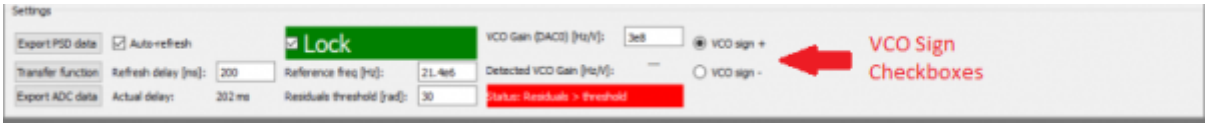

Fig. 19: Location of the VCO Sign Checkboxes, and the "Lock" button.

Once a lock has been obtained, the green plot of phase noise on the “Phase Noise PSD, std dev =” plot will show a dramatic reduction in noise from ƒCEO's unlocked state. This number is a good characterization of the stability of your lock. A good lock of ƒCEO is indicated by a std_dev less than 2 rad, but this value can be pushed down even further by optimizing the PID settings of the FFC-CM.

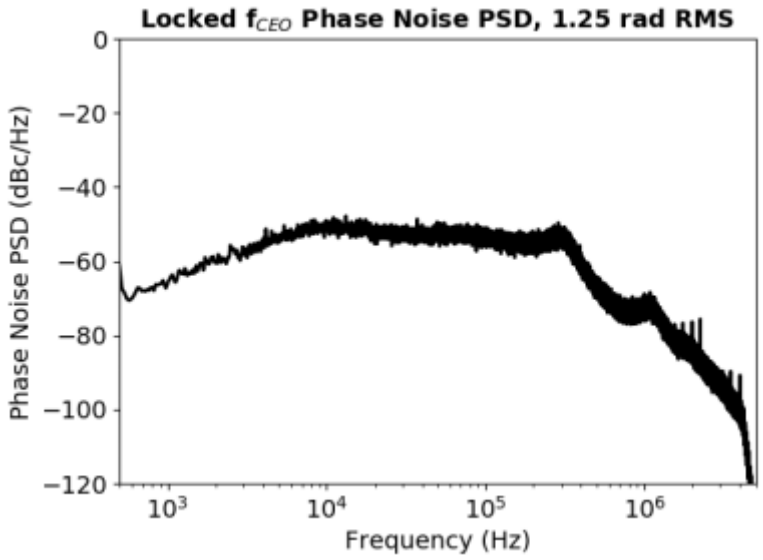

Fig. 20: f_CEO Phase Noise Example

After obtaining a lock, it is possible to change the lock frequency using the “Reference freq [Hz]:” field in the FPGA GUI. To do so, unlock f_{CEO}, then change the value of “Reference freq [Hz]:” and relock the FFC-CM. If you do not unlock the laser first, you will likely rail the modulation output.

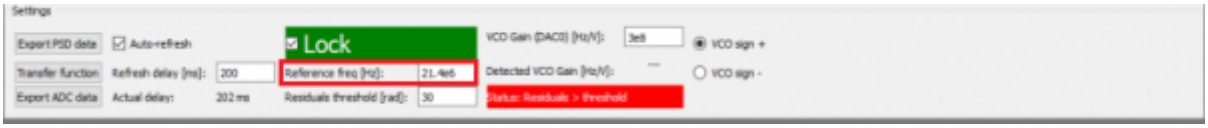

Fig. 21: Location of the "Reference freq [Hz]:" field

Step 9: Optical Lock

The process for locking f_{opt} is nearly identical to locking f_{CEO}, except that there is an extra slider (Offset DAC 2) on the screen. It has no effect on the system, and can be left alone. Begin by adjusting the “Offset DAC 1 [V]” slider until the beatnote is centered within the red bandpass filter spectrum. Check for the VCO sign by adjusting the “Offset DAC 1 [V]” slider as described in Step 8, check the appropriate VCO sign box, then check the “Lock” checkbox at the top of the tab and wait a moment. The Phase Noise PSD plot will indicate whether your system is locked by showing a dramatic reduction in noise, and standard deviation. If your system is railing, change your VCO sign by selecting the opposite “VCO sign” checkbox to the right of the “Lock” checkbox. To optimize your lock, follow the instructions for optimizing the PID settings of the FFC-CM. As with f_{CEO}, the lock frequency can be changed using the “Reference freq [Hz]:” field in the FPGA GUI. Once again, this should be done while the system is unlocked.

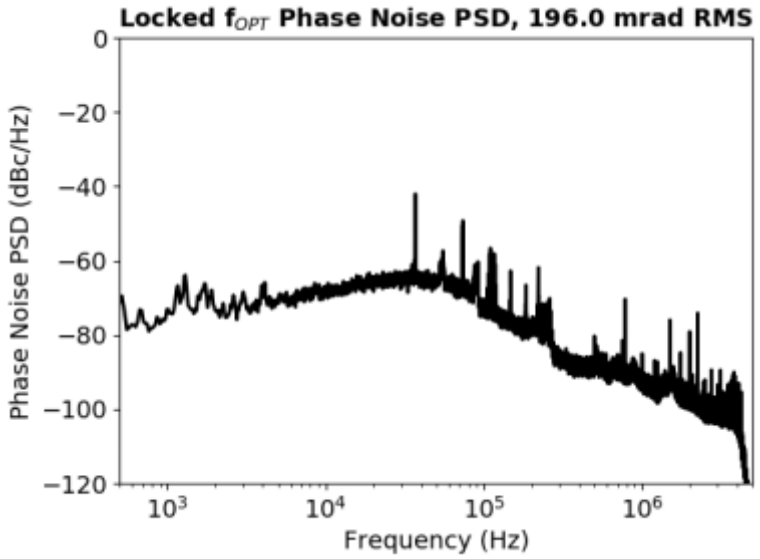

Fig. 22: f_opt Phase Noise Example

Optimizing FPGA PID Locking Parameters

The PID parameters provided in your CoC describe a baseline for a good lock of the FFC-CM to a reference laser. However, these parameters are system dependent, and can likely be optimized further to obtain a better lock than the CoC settings. To optimize the PID parameters for your system, begin by selecting the Proportional Gain slider “Kp” and moving it left or right with the arrow keys on your keyboard. Watch for the number displayed by std_dev in the phase noise plot to decrease, and move the slider until the std_dev has reached a minimum. Next, repeat this process for each slider. If for some reason your system comes unlocked during this process, simply reset the PID parameters to those found in your CoC and start again.

Slow Loop Feedback

The Slow Loop feature allows the user to enable a slow servo temperature control of the intracavity PZT to prevent offset drift over long periods of time. It is recommended to always enable this feature after setting up a lock, as without it the PZT's offset voltage can drift to its rails over the course of several hours or even less. To enable the Slow Loop feature, close all other serial terminals communicating with the FFC-CM, then navigate to the Slow Loop tab in the menu bar of the FPGA software, fill in the “FFC COM Port:” field with the number corresponding to your FFC-CM's COM port, choose the desired setpoint of the PZT, and press the “Activate Temperature Slow Loop” button at the top of the tab. For example, if your FPGA is on COM4, and your FFC-CM is on COM8, type “8” into the “FFC Com Port:” field and then press the button. This will bring up a command prompt window which will display information about the Slow Loop, such as the cavity temperature, and the current PZT setpoint. In general, it is best to select a setpoint near the center of the PZT's available range.

The Slow Loop Servo uses the serial COM port on the FFC-CM, and as such will not work if that port is being used by another command interface such as Tera Term. Make sure that all other serial command interfaces are closed before trying to enable the slow loop feature.

FAQ